Designer's Handbook

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1. INTRODUCTION

1.1. OPTIMUM DESIGN: Mission Statement

1.1.1. Our company's mission statement sets the tone for the business. It communicates how we perceive ourselves and our position in the marketplace. It also guides us in our long-term goals, being revised from time to time to meet changing circumstances.

1.1.2. We perceive ourselves as a high-quality provider of engineering services, and our mission statement reflects that perception. Every employee, whether a designer or not, should keep this in mind as we perform our various tasks, since all facets of the organization affect every other part.

1.1.2.1. *Optimum Design Associates (OPTIMUM)* provides consistent, accurate engineering support services to electronics firms, focusing primarily on Printed Circuit Board engineering and design.

1.1.2.2. *OPTIMUM* will respond to its customers' evolving needs resulting from changing technology, business restructuring, and other influences.

1.1.2.3. *OPTIMUM* will use the best available tools for the job that are consistent with high quality and quick turnaround times.

1.1.2.4. *OPTIMUM* is committed to Total Quality Management. Design decisions are evaluated in light of their effect on the processes that follow it—Fabrication, Assembly and Test. To accomplish our TQM goals, *OPTIMUM* will maintain professional relationships with the other vendors that comprise the manufacturing chain.

1.1.2.5. *OPTIMUM* will assist each of its designers and other employees in their professional development so that they attain and maintain the highest levels of competency in the industry.

1.2. Scope and Purpose

1.2.1. This document establishes a set of basic design criteria and process flows to use for all ODA PCB designs. These criteria represent the minimum quality standards that each board should meet.

1.2.2. The intended reader will be familiar with the design process, and will have designed several boards from start to finish. This material is not intended to be training material for those getting into design work. However, much useful information may be gained from it by anyone needing to know more about how to correctly design printed circuit boards.

1.2.3. Since ODA is a design service bureau, its customers' requirements will take precedence in all cases where they differ from these guidelines. However, if customers make design requests that are clearly inferior to the methods presented here, it is the designer's job to persuade the customer to accept the better alternative, if possible. Any persuasion should be done in the spirit of helpfulness, and clearly for the purpose of providing better service to the customer. Argumentation is to be avoided.

1.2.4. Use of this design standard will result in manufacturable PC assemblies that can be produced at a wide range of fabrication and assembly houses.

1.3. Overview

1.3.1. Every complex process needs guidelines in order to be performed properly. Printed circuit board design is, without doubt, a complex process. And in this day of increased

competition, businesses that produce high-tech electronic products cannot afford to spend time and money working with inferior PC design bureaus. In order for ODA to survive and prosper, the quality of its product, in every respect, must be high and remain so. We cannot afford to lose even *one customer* due to negligence. This is the driving force behind these guidelines.

1.3.2. This document specifically aims to increase or maintain each ODA designer's accuracy and consistency, and to maintain the repeatability of each ODA design. These concepts are briefly described in the following paragraphs.

1.3.3. Accuracy

1.3.3.1. The evaluation of an individual board design is its accuracy—that is, how well it conforms to the stated requirements of the customer. Are all nets routed? Without shorts or opens? In accordance with all routing parameters? Is the board dimensionally correct? Are mechanically defined components in their proper place? Have all rules been followed? Since a vast majority of the designs are considered prototypes, engineers should not have to contend with layout errors when debugging these untested circuits.

1.3.3.2. Accuracy also extends to the details of documentation. As a service bureau, our designs may be electrically perfect, but our customers will long remember if we misspell their company name in the title block, or if we put the wrong number on the assembly drawing. ODA is committed to the goal of creating designs and documentation that are 100% correct.

1.3.4. Consistency

1.3.4.1. Consistency is the degree to which different designs, made at different times and by different designers, have the same "look and feel." For instance, parts are constructed in a similar manner with respect to such things as silkscreen, orientation, and placement of information on consistent layers. Also, the methods of documenting the design should not vary from board to board – reference designator location and orientation, fabrication drawing notes, deliverables – all should have a consistency, no matter when the job was completed, nor by whom. The packages produced by ODA should be highly consistent with each other.

1.3.5. Repeatability (Paper Trail)

1.3.5.1. The course of any given project may include performing one or more steps multiple times. For example, netlists may be compiled several times; Parts may be imported more than once; Boards may be re-routed multiple times. In each step of the process, the designer may take unique actions that are necessary to complete the board. If, for some reason, the design is re-started, or a step is repeated, then those unique actions must also be re-done. For this reason ODA uses the combination of the ODA Project Checklist and the ODA Project Black Book to keep track of important information needed to be passed along from one designer to another, as well as from one revision to the next.

1.3.5.2. The ODA Project Checklist file is a Microsoft Excel spreadsheet (`Project Checklist.xls`) located within each unique project directory and is split into three sheets: Board Information, ODA Job Checklist, and ODA ECO Checklist. The Board Information sheet contains contact information, project data (board name, fabrication and assembly numbers), milestones, designer notes, and net changes. It is the designer's responsibility to ensure that any pertinent design information be recorded on this sheet. The checklist sheets contain a variety of important details that must be incorporated or considered within the design

process of laying out a board. It is imperative and required by ODA management that all detail items of the checklist be thoughtfully considered and incorporated if deemed necessary per ODA standards or submitted client standards. A check mark next to the detailed item states that the designer has thoughtfully considered or incorporated the item and thus all items should be checked off by the end of the design process.

1.3.5.3. The ODA Black Book is simply a black folder used to hold all hard copy materials supplied by the client (schematics, bills of material, guidelines, placement floorplans, mechanicals, etc.) as well as anything else deemed important by the designer working on that particular project. Any information no longer relevant to the design shall be marked as "HISTORY".

1.3.6. The Structure of these Guidelines

This Design Book is divided into three major sections: The *Design Process Description, Tool-Specific Information and Special Topics,* and *Designer's Reference Material*.

1.3.6.1. Design Process Description

1.3.6.1.1. Using the stages of the design process as an outline, the various considerations and requirements of PC design are described. This is a general discussion of PC design, without reference to any specific tool, such as Expedition, PADS, or Allegro.

1.3.6.2. Tool-Specific Information and Special Topics

1.3.6.2.1. The design process is not just a concept; PC boards are designed with a tool. Therefore, some discussion is necessary regarding the processes and procedures that the various tools follow. Since this is not a tutorial in how to design a PCB with, say, Mentor Graphics software, not all stages of the design process are documented. But some topics will require a more concrete explanation of how to perform certain tasks using a particular tool.

1.3.6.2.2. In addition to tool-specific information, there are some special topics that deserve individual consideration. These special topics are also included in this section.

1.3.6.3. Designer's Reference Material

1.3.6.3.1. Time has proven that a designer needs a rather wide range of knowledge in order to produce good results. This section collects various tables, graphs, drawings, lists and formulae that are basic tools that one needs from time to time. Additional reference material may become necessary as technology changes the way design work is done, so you are encouraged to append it to this book whenever the need arises.

1.3.6.3.2. Some material is customer-specific. That is why this Design Book is provided in a three-ring binder. At the end is a section for collecting specifications according to customer.

THE LAYOUT PROCESS

2. Stages in the Design Process

The following stages in the design process provide the outline for the discussion that follows:

- Initial Design Review
- Parts Creation
- Integration
- Pre-Layout Interview
- Mechanical Definition
- Placement/Review
- Pin Swapping
- Via Patterns
- Power/Ground Routing
- Critical Signals
- Review Critical Lines
- Routing
- Cleanup
- Pre-Delivery Review
- Final Edits
- Final Extract
- Create Deliverables
- DFM Check
- Archive Job

2.1. Initial Design Review

2.1.1. Before starting the design of a PC board, much preliminary information must be gathered and assembled into a consistent package. The purpose of the Initial Design Review step is to get most of this preliminary information in an orderly, complete way. Performing this step properly will make every following step that much easier, regardless of who works on them or how long ago the project was designed.

2.2. Parts Creation

2.2.1. The fundamental building blocks for a design are the parts and shapes that are placed on the board. The parts must be made according to both the manufacturer's specifications and ODA Library Standards document. And although many other aspects of the design can be verified using automated tools (e.g., DRC), parts cannot be checked with automated tools. This means that it is critical to make parts that are correct in every respect. An incorrectly made part could go undetected through the entire process, and only when the fabricated board is being assembled, or even later in test, would the error be found out.

2.2.2. Parts creation is normally performed by the Librarian, however, each designer needs to be familiar with the process, in case of emergency, when the Librarian might be unavailable.

2.2.3. The parts creation process involves three elements: Footprints (including padstack), Symbols, and the Parts Database. The first step in the parts creation process is to determine the cell to be used. The library is checked to see if an existing cell can be used for the part and if not, a new cell is created in accordance with ODA cell creation standards. It is also possible that some new padstacks will also be required at this point.

2.2.4. The second step in the parts creation process is to determine the symbol to be used. The library is checked to see if an existing symbol can be used for the part and if not, a

new symbol is created in accordance with ODA symbol creation standards. Note: If the design is netlist driven, a symbol is not necessary.

2.2.5. The third and last step is to create a PDB (Parts Database) entry for the part. This involves importing both the cell and the symbol and then mapping the pins (including pin and gate swappability) on each so that the schematic symbol is in sync with the cell used in the PCB design. Properties that are to be used in design outputs, such as Bills of Materials and simulation files, are also entered into the PDB.

2.2.6. The use of properly constructed PDBs will ensure a seamless transition of the design from schematic entry through PCB layout.

2.3. Integration

2.3.1. Integration is the process of adding intelligence to the PCB database by means of a netlist or schematic. This can only occur once all of the necessary library elements for a particular design have been created by ODA or by receiving a customer-supplied library. A 100% successful design integration (no errors) will allow the designer to confidently place components, route, and output manufacturing files with the PCB database and schematic in sync.

2.3.2. The engineer may supply the data for integration in one of two ways: Schematic or Netlist.

2.3.3. Schematic

2.3.3.1. Integrating a schematic to a PCB can typically only be done within the same EDA product family, with the exception of a few third-party schematic entry tools. For the most part, they all work the same, in that an intermediate file is created and is read in by both schematic and PCB tool. The advantages of schematic integration over netlist integration are that schematic integration allows for cross-probing, easy forward- and back-annotation, and easy pass through of net properties from the engineer to the designer.

2.3.4. Netlist

2.3.4.1. For the most part, integration by netlist is still the most common form of input that we see today. Because netlists come in many different formats, custom changes to the netlist will most likely be necessary before integrating with a PCB file. Netlists submitted to ODA, must be translated (reformatted) into the proper format of the EDA tool to be used. Translate the netlist by using a Word™ macro or a third-party netlist converter (e.g., Omninet®). In most cases, the parts list section of the netlist will need to be retyped based on the part name assigned within the PCB tool. Please see the Reference section for sample netlist formats used at ODA.

2.3.4.2. In some cases, it may be necessary to edit the customer-supplied netlist to ensure a successful integration (no errors). An area is supplied within the Project Checkoff List to document all changes made to the netlist. This is a mandatory and important step to ensure repeatability for that design now and for future revisions. Below are a few sample reasons to make a netlist change:

Pin Number Changes The words, “Anode” and “Cathode” used as pin #’s, whereas our footprint uses pin numbers 1 and 2

Pin Number Deletes In some EDA tools, plated mounting holes for components don’t require a pin number and thus should not be included in the netlist. Please be sure to document this in the designer notes section of the Project Checkoff List to ensure that the

mounting hole's net connection gets added back in within the PCB.

Netname Deletes In a few capture tools the net name "NOCONNECT" clumps all unconnected pins together. In this case delete this entire net.

Netname format Some EDA netlist formats don't allow certain characters and must be changed (e.g., the backslashes ("\") must be changed to the underscores ("_") for a Mentor Expedition netlist). See SPECIAL TOPICS for more specifics.

2.3.4.3. As a rule, try to keep the number of netlist changes to a minimum by asking the engineer to make changes on the schematic or by changing the footprint to match the netlist.

2.4. Pre-Layout Interview

2.4.1. It is important for the board designer and the design engineer to discuss the design as early as possible in the board layout process. Often many things are assumed by the engineer, because of one's closeness and familiarity with the design, which would never be communicated to the board designer until it is too late. This early discussion will likely save time by eliminating the need for reworking sections of the design caused by the designer not being aware of the engineer's intentions.

2.4.2. The Pre-Layout Interview is also important for establishing a rapport between design engineer and board designer so the engineer can feel more comfortable in leaving design decisions to the ODA designer.

2.4.3. In order to provide a basis for the meeting, and to assure that little (if anything) is left out of the discussion, use the "ODA PCB Design Specification" form (a separate document). In it you will find questions regarding such things as the mechanical data that should be supplied, the customer's requirements for documentation, routing information, critical signals, fanout preferences, etc.

2.4.4. The following abbreviated list shows you some areas of concern at this early stage of the design.

2.4.4.1. INTERVIEW CHECKLIST

2.4.4.1.1. **Mechanical**

2.4.4.1.1.1. Mechanical spec hard copy or in DXF

2.4.4.1.1.2. For large boards are stiffeners required

2.4.4.1.1.3. Maximum thickness

2.4.4.1.1.4. Mounting holes plated / unplated. Plated holes to be tied to what net?

2.4.4.1.1.5. Fixed component locations

2.4.4.1.1.6. Place / route obstructs, including height restrictions

2.4.4.1.1.7. Board laminate material, FR-4, FR-406, 4003, etc

2.4.4.1.2. **Placement**

2.4.4.1.2.1. Floor plan available

2.4.4.1.2.2. Thermal considerations, heatsinks location and orientation, temperature sensitive components

2.4.4.1.2.3. Bypassing components assigned, rules per device

2.4.4.1.2.4. Termination components present, optimal placement criteria for terminations

2.4.4.1.2.5. Clearance requirements around connectors for mating half

2.4.4.1.2.6. Use of component tie downs if board is for high vibration environment, like avionics

2.4.4.1.2.7. RF shielding used? Identification of sensitive circuit areas.

2.4.4.1.2.8. Are there any high voltage areas, circuits requiring electrical isolation?

2.4.4.1.3. **Routing**

2.4.4.1.3.1. Layer count

2.4.4.1.3.2. Board stackup defined by ODA, Customer, or fabrication shop (preferred)

2.4.4.1.3.3. Controlled impedance requirements

2.4.4.1.3.4. Critical net routing and clearances defined

2.4.4.1.3.5. Route strategies for specific circuit types, JTAG, Busses, LVDS, differential pairs, analog, and power

2.4.4.1.3.6. If differential pairs exist, edge coupled or broadside?

2.4.4.1.3.7. Plane assignments per layer, split planes allowed, local planes for specific devices.

2.4.4.1.3.8. Via wall required sensitive areas

2.4.4.1.3.9. SMT in power circuits buried or thermal ties to surface planes

2.4.4.1.4. **Misc.**

2.4.4.1.4.1. ICT or flying probe required, preferred and minimum spacing

2.4.4.1.4.2. Renumber reference designators required

2.4.4.1.4.3. Reference designators visible on silk for high density designs

2.4.4.1.4.4. Silkscreen and etch text requirements (fabrication and assembly numbers)

2.4.4.1.4.5. Silkscreen functional labels for connectors, switches, jumpers, and LED's

2.4.4.1.4.6. Fabrication, assembly, and artworks numbers for board drawings

2.5. Mechanical Definition

2.5.1. The mechanical definition stage is where the outline of the board is defined. All design tools require the completion of this step before placing any parts. But mechanical definition includes many more items than just the board outline. These include defining keep-in/keep-out areas, placement of origins for the board and the drill, the location of tooling and mounting holes, global fiducials, mechanically defined parts, and breakaway rails.

2.5.2. Please note that the mechanical entry process is much like the library entry process, being critical that it be done accurately and, if done wrong, could render the manufactured board useless. For instance, there is no automatic checking to ensure that the board outline is drawn properly. So the board could be drawn slightly larger or smaller than specified, resulting in a sub-assembly that will not fit into the space

provided by the device's packaging. Because of this, **all** items in the mechanical definition must be verified to be correct before the design process can continue.

2.5.3. This section describes the board outline, and other items that may be required during mechanical definition.

2.5.4. Board outline

2.5.4.1. At ODA the board outline is a true representation of the shape of the board. This includes all arcs and angles that are part of the finished board after being fabricated. All board outlines are drawn with a 5-mil line. Board outlines are supplied by the customer in one of the following formats (listed by priority of preference):

2.5.4.2. **DXF** is a standard Autocad™ output file, which contains the board outline as well as possibly mechanically-defined components, cutouts, keepout, and mounting holes, all of which can be read directly into all EDA tools onto a draft layer for reference. The board outline can be converted from the draft layer to become the actual system board outline, thus eliminating the need for checking.

2.5.4.3. **IDF** is a standard Solid Works™ output file, which works much like the DXF file, except that mechanical data is not read onto a draft layer, but is automatically converted to the correct system-defined elements. For EDA tools that support this input, it would be the preferred input file.

2.5.4.4. **Hand drawn sketches** have become less common over the years, but are still used for mechanical input. Be sure to accurately input the dimensions onto the board outline layer. In addition to double checking your work, be sure to send a dimensioned mechanical drawing back to the engineer for review and approval.

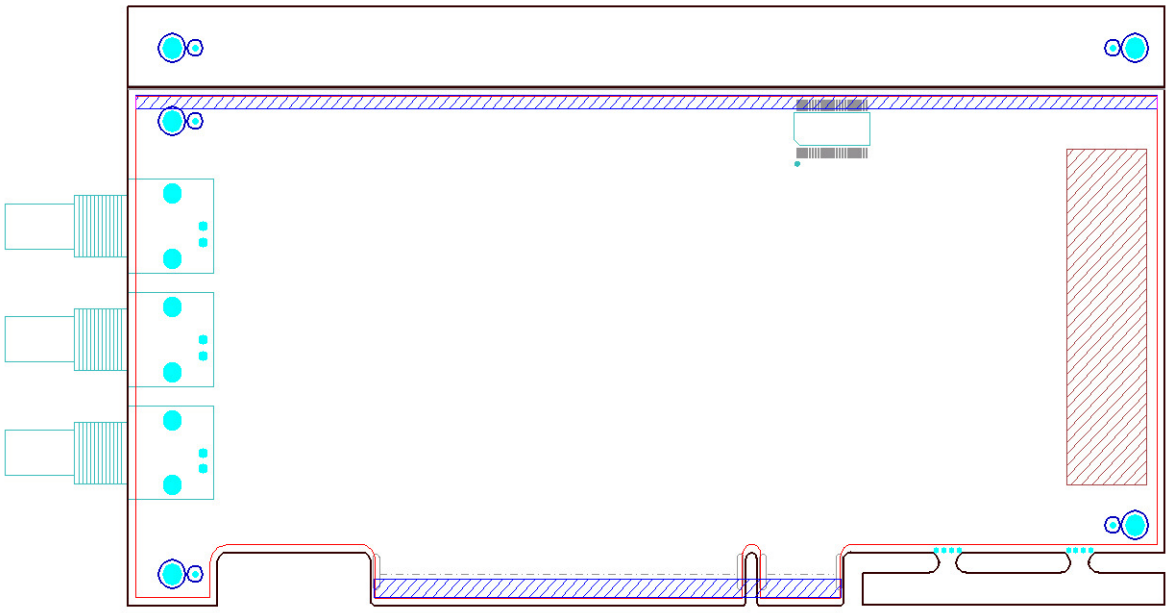


Figure 1: Mechanical Definition

2.5.5. Keep-in/Keep-out Areas

2.5.5.1. The keep-in/keep-out areas are geometric shapes that define limits to where design elements may be located. A keep-in area is an inclusion shape, within

which the design elements must be located. A keep-out area is an exclusion shape, which restricts elements from being placed inside. The elements being restricted are traces and components. Designers must add these specified areas from the mechanical documentation received from the customer. Most EDA tools have specifically-defined layers on which these area shapes reside.

2.5.5.2. The keep-in area is also commonly known as the Route Border, an area within which all routes, vias, and planes must be located. The route border should be cleared from the board outline, including all cutouts, by .050" (.040" min.) on the outer layers, and .025" (.020" min.) on the inner layers. **Figure 1** shows the route border in red.

2.5.5.3. Also in **Figure 1** are keep-out areas for tooling holes and global fiducials. These keep-outs restrict traces and vias from entering. Keep-outs are also defined for components in the blue crosshatched areas. Please refer to the "Fiducials," "Tooling and Mounting Holes," and "Breakaway Rails" sections for more information.

2.5.6. Board and Drill Origins

2.5.6.1. Board and NC Drill origins are to be placed at the bottom left tooling hole to coincide with the 0,0 fabrication drawing dimension. Be sure to define the origin before components or routes are placed, in order to eliminate any inconsistencies in the placement, via, or routing grids. See **Figure 2**.

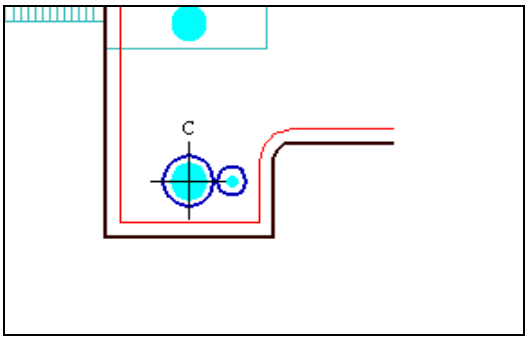


Figure 2: Board and Drill Origins

2.5.7. Tooling and Mounting Holes

2.5.7.1. All boards must have at least three tooling holes for use in fabrication and assembly. The preferred arrangement is shown in **Figure 1**. Tooling holes must be non-plated and .125" in size. If the customer-supplied mechanical drawing has non-plated mounting holes specified in the corners that are .100"-.200" in diameter, these may be used in place of tooling holes.

2.5.7.2. If a mounting hole is to be plated through, then ask the engineer if they are to be tied to any specific net (e.g., CGND). The engineer must also determine what size clearance to components and routes are needed due to hardware requirements (see APPENDIX I: NUT/BOLT SIZES AND CLEARANCES in the Reference Material section).

2.5.7.3. **Note:** All non-plated holes (mounting. or tooling) must have a .012"/.025" min./preferred route obstruct on all layers. Double check your work to make sure that mounting holes are accurately placed per the mechanical input.

2.5.8. Fiducials

2.5.8.1. If a board has surface-mounted components, then the board must also have three global fiducials (.040″ round pad with a .100″ soldermask clearance). These global fiducials must be located in the same configuration as the tooling holes previously mentioned (see **Figure 1**), and be included on any outer layer (top or bottom) that has surface-mounted components.

2.5.8.2. No component, via, or trace is allowed inside the .100" fiducial clearance area. You may need to specifically add keep-out shapes around all fiducials in order to accomplish this.

2.5.9. Mechanically-Defined Components

2.5.9.1. Typically, most boards will have a small number of parts that must be located exactly per the supplied mechanical input. These are the mechanically-defined components. Be sure to place these accurately and to lock them down.

2.5.9.2. Do not locate these parts by using coordinates unless you have verified that the part origin is in the same location as the locating coordinates in the mechanical drawing. For example, if a through-hole part has its origin defined as Pin 1, and the mechanical drawing uses the part's mounting hole to locate the part, then you cannot place the part by setting its location to the drawing's coordinates.

2.5.10. Breakaway Rails

2.5.10.1. Designers must be aware that the customer-supplied board outline shape isn't always necessarily the shape that is to be delivered to the fabrication and assembly house for manufacturing. PCB's must have two parallel sides (preferably the two longest sides) for processing them through the assembly equipment (conveyor transport).

2.5.10.2. Breakaway rails can be used to accommodate a variety of odd board shapes (see **Figure 1**). The other reason to use breakaway rails is to create the necessary clearance from component to board edge (see **Figure 1**). As a general rule, top side components must be clear from the two long sides of the board outline by .120" (3mm) and bottom side components cleared by .200" (5mm). If this condition can't be met, then the designer must add either 1 or 2 rails as necessary.

2.5.10.3. Breakaways can be accomplished by either using routed slots along with a series of "mouse bites" (see **Figure 3**) or by a V-grove scoring of the board (see **Figure 4**). If a breakaway rail is needed along an entirely straight edge, ODA's preferred breakaway would be to use V-grove scoring. For all other cases, use slots with mouse bites.

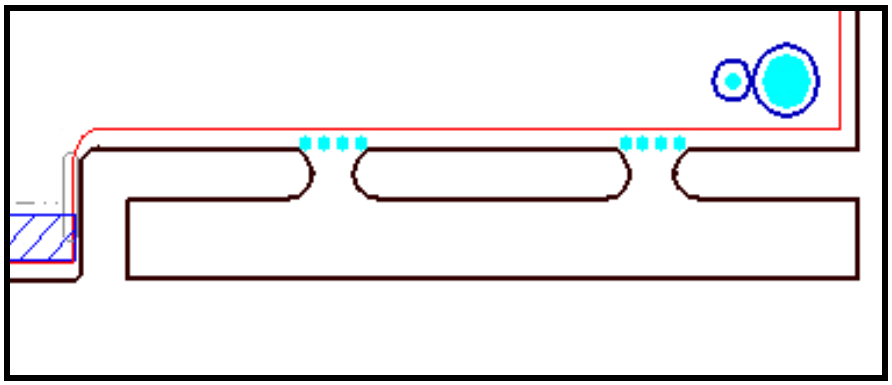


Figure 3: Mousebites

2.5.10.4. Breakaway rails that are added only for increasing component–to-board-edge clearances are to be at least .500". These rails should also include fiducials and a .125" non-plated tooling hole in each corner (see **Figure 1**). The component at the top edge of the board may violate the component keep-out area shown because the added v-groove breakaway rail allows the board to be fabricated and assembled with proper clearances. Please note that if the board will be part of a sub-panel assembly, rails are not necessary, since the sub-panel will have the rails. Rails take up material and thus add cost.

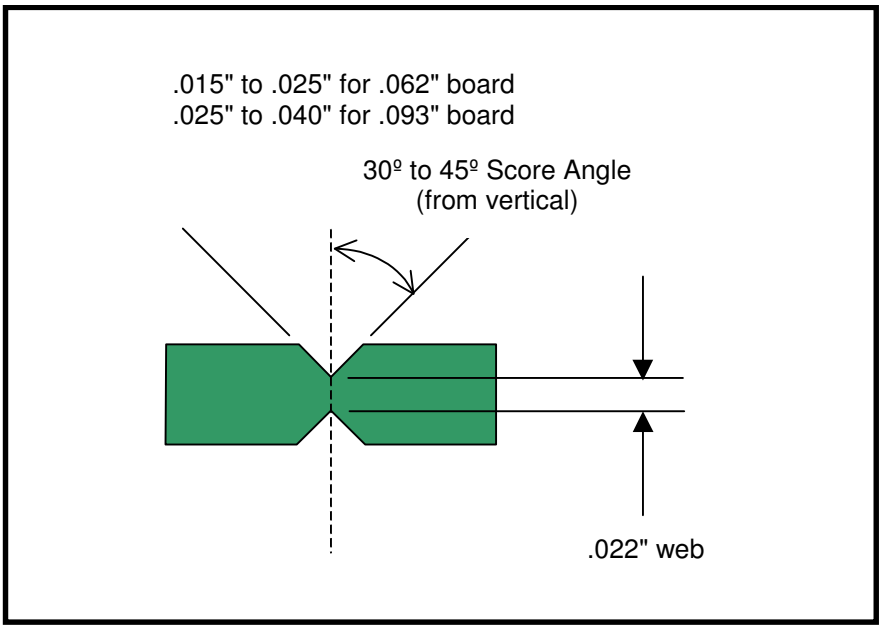


Figure 4: Breakaway Rails

2.5.11. ECO

2.5.11.1. In the course of a new design, or during a revision of an old design, the customer may change the mechanical definition of the board in whole or in part. In the case of such changes, be sure to use the defined process discussed in this section to ensure that all changes are incorporated properly.

2.5.12. ODA Project Checklist (Mechanical Section)

2.5.12.1. At this point, all Mechanical items within the ODA Project Checklist spreadsheet should be marked off (marked off means done or considered).

2.6. Placement

2.6.1. Although all phases of the design process are important, the placement phase at ODA is probably the most important and most time consuming part of the design flow. A successful placement will not only meet the complex electrical specifications, but will also meet all manufacturing requirements. This section consists of the following two sub-sections–

2.6.1.1. Placement: Electrical
2.6.1.2. Placement: Manufacturing

2.6.2. Placement: Electrical

2.6.2.1. The more that the designer can understand about a particular circuit, the better placement and routes will result. It is extremely important that ODA designers be able to recognize particular types of circuits and make appropriate decisions regarding placement. If your knowledge of circuits needs improvement, then be diligent to ask questions regarding the schematics that you work on, and become increasingly informed about their treatment in a design.

2.6.2.2. Overview of Electrical Placement

2.6.2.2.1. Experience has shown that the placement process is best accomplished by following a logical progression. The following steps describe this progression, and, with rare exception, should be adhered to:

2.6.2.2.1.1.	**Design Review**	In this step, the designer becomes very familiar with the schematic, the floorplan (if provided), net rules, and any component manufacturers' application notes.
2.6.2.2.1.2.	**Place Fixed Components**	Since you have no control over the placement of mechanically defined components, these are the first that should be put on the board.
2.6.2.2.1.3.	**Place Interface Components**	These are typically a group of components (such as an ethernet circuit) that has inputs or outputs tied to either connectors, fingers, headers, or other off-board sources or destinations.
2.6.2.2.1.4.	**Place Main Active Components**	These are the main components, such as processors, FPGAs, etc., that many other components will be near to.
2.6.2.2.1.5.	**Place Misc. Active Components**	Clocks, buffers, memory, and all other IC's should be placed at this time. It is also OK at this point to place critical circuits, such as a power supply or analog devices.
2.6.2.2.1.6.	**General Placement Review**	At this time send over a placement to the engineer to ensure that you are moving

		in the right direction. Be sure to clean up the reference designator text before sending it out to the engineer.
2.6.2.2.1.7.	**Place the Rest of the Components**	After you receive approval from the engineer to proceed, go ahead and place the rest of the passive components.
2.6.2.2.1.8.	**Final Placement Review**	Once all components have been placed, reference designator text is readable, board has been reviewed for manufacturability and test, then send the placement off to the engineer for final placement review. At this point all details regarding mechanical and placement within the ODA Project Checklist have been checked off.

2.6.2.3. Schematic / Rats

2.6.2.3.1. The placement process should be guided by the schematic, not by net lines drawn on the screen. Seasoned designers are very familiar with how important a schematic is to a successful placement. Over time many designers take a shortcut by placing components according to the tool-generated net lines (rats) exclusively. However, at ODA the schematic remains the primary aid in placing components, while the use of “rats” during placement is secondary.

2.6.2.3.2. Prior to starting a design, spend plenty of time understanding how the schematic is organized. It is important to establish placement “flow” prior to starting component placement. Typically, engineers will layout the schematic in such a way that the circuit layout will be logical, and the “flow” obvious. However, in some cases, either through the overuse of hierarchy or through crowding too much circuitry on each page, the “flow” is hard to grasp. In such a case, you may need a pre-layout conceptual drawing from the engineer in the form of a “floorplan,” which is discussed in the following section.

2.6.2.4. Floorplan

2.6.2.4.1. A “floorplan” is a drawing that indicates general areas where blocks of circuitry are to be placed on the board. These areas (continuing the architectural metaphor) are called “rooms.” Floorplans bridge the gap between the schematic drawing and the physical layout. This gives the designer a head start on placement.

2.6.2.4.2. The floorplan can be communicated by two different means. It is either an integrated CAD (Computer Automated Design) tool function, or it is an electronic or physical illustration. The first is a complex floorplan in a CAD tool that defines allowable placement ‘rooms’ for specific areas of circuitry, incorporating place, height and route type obstructs, as applicable. This sets up DRC guidelines and rules for the designer to follow and the CAD tool to verify against.

2.6.2.4.3. The second meaning of floorplanning is where the engineer provides the PCB designer with an overview of an expected placement and routing flow. This is the type of floorplanning discussed here.

2.6.2.4.4. Do not underestimate the usefulness of a floorplan. If a PCB layout job begins without an idea as to how the engineer expects the placement to look, then a lot of time may be wasted placing and re-placing components until it is accepted by the engineer.

2.6.2.4.5. The drawing should include a board outline (not necessarily dimensioned), an indication of where to place I/O connectors, and a series of rooms for placement of circuit blocks. It is helpful if these rooms have the relevant schematic sheet numbers for the circuits they contain, as it makes it a lot easier to find things on a 100-plus page schematic if you know where to look.

2.6.2.4.6. The drawing could also show some sort of signal path flow. This helps in knowing where the signals entering and exiting a room are coming from or going to, making sensible placement of components within the room a lot easier.

2.6.2.4.7. A simple floorplan drawing, as illustrated above (**Figure 5**), tells the designer immediately how to start component placement. The rooms may change in size, shape and possibly even relative position, but the PCB designer can make this change with confidence because the signal flow is indicated and can be taken into account when reorganizing the rooms. The schematic sheet numbers will make finding the parts a lot easier.

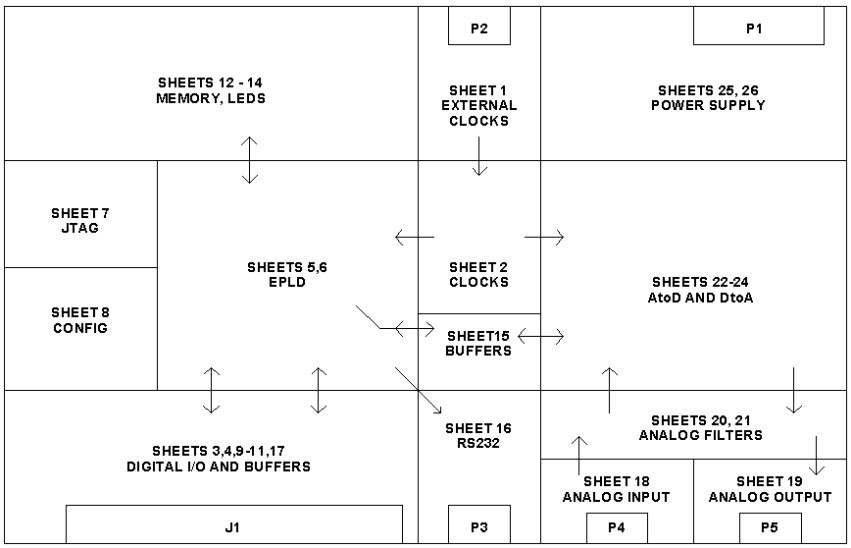


Figure 5: Example of Pre-Layout Conceptual Floorplan

2.6.2.5. Mechanically-Defined Components

2.6.2.5.1. Typically, boards will have a small number of parts that must be located exactly per customer-supplied mechanical input. These are the mechanically-defined components. Be sure to place them accurately, and to lock them down so they do not accidentally change position.

2.6.2.5.2. Do not locate these parts by using coordinates unless you have verified that the part origin is in the same location as the locating coordinates in the mechanical drawing. For example, if a through-hole part has its origin defined as Pin 1, and the mechanical drawing uses the part's mounting hole to locate the part, then you cannot place the part by setting its location to the drawing's coordinates.

2.6.2.6. Timing Considerations

2.6.2.6.1. In high-speed designs that have a heavy amount of timing constraints, it is very important for the designer to become very familiar with the timing issues and their impact on the placement process. Busses may have either maximum length constraints or minimum length constraints. Busses that have maximum length constraints placed upon them will certainly restrict the distance from one component to another, and conversely, busses with minimum length constraints, or delay formulas, would require placing components further away from each other.

2.6.2.6.2. Most EDA tools allow for timing constraints to be entered as a Net Property to aid the designer in making proper placement decisions. Of course, it is absolutely best to get all timing considerations up-front in the design process for the greatest effect.

2.6.2.6.3. Even with the best of all possible placements, however, some traces will need to be adjusted to make them the proper length to meet the required timing considerations. Most traces are modified using a serpentine routing pattern, which is further explained and illustrated in the Routing section.

2.6.2.7. Component Manufacturer's Application Notes or Reference Designs

2.6.2.7.1. Today it is very common for an engineer to require that a specific circuit or circuits within a design be layed out per the Component Manufacturer's Application Notes (App. Note) or Reference Design. It is a growing trend for IC chip manufacturers to provide App. Notes to ensure that their chips will work as intended. The App. Note may be as simple as a layout note on how to properly bypass the component, or as complex as providing detailed placement and routing instructions in the form of graphics or other electronic files, such as Gerbers. If you are unfamiliar with a particular IC and were not given any specific layout instructions by the engineer, it is your responsibility to search the IC manufacturer's website for any relevant layout instructions.

2.6.2.8. Bypassing / Decoupling Capacitors

2.6.2.8.1. The placement of bypass capacitors is one of the most critical phases of the design process. Failure to place them correctly can completely negate their performance. Also critical is a situation in which there are too few capacitors for particular components. This information should be communicated back to the engineer, whenever it occurs, so that the schematic can be updated.

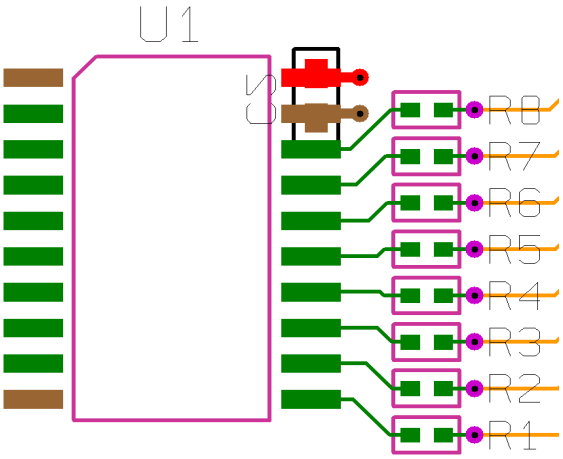


Figure 6: Capacitor on Opposite Side

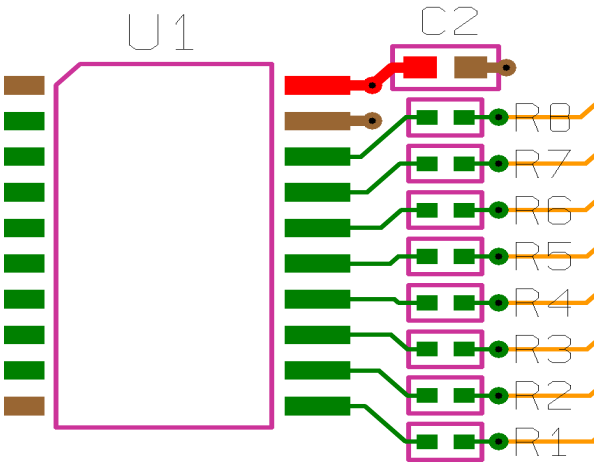


Figure 7: Capacitor on Same Side

2.6.2.8.2. The major factor in determining where to place the bypass capacitors is whether components can be placed on the bottom side of the board. It is much better if they can, because then the capacitors can usually be placed under the pads of top-side SMT components. Placing them on the bottom side usually frees up more space for fanout traces and vias. If capacitors must be placed on the top side, then they should be located as closely as practicable to the power pins of the components.

2.6.2.8.3. Notice in **Figure 7** that the bypass capacitor takes up additional space on the top side and therefore reduces the available space for vias. In **Figure 6**, however, because the capacitor is on the opposite side, we can place it where the pads of the capacitor are directly underneath the pads of the IC on top. This space could not be used for vias, so we have not lost any via space.

2.6.2.8.4. There are differing opinions among engineers regarding how the power traces should be routed to the bypass capacitor. Some engineers insist that the trace first connect the device pin to the capacitor and only then go on to the power plane via **(Figure 7)**.

2.6.2.8.5. Other engineers say that either of the two methods shown in **Figure 6** and **Figure 7** is more than adequate, and that the placement of the power via with respect to the capacitor land is irrelevant.

2.6.2.8.6. ODA will use either of these two illustrated methods unless specifically instructed to do otherwise by the engineer. But of the two methods shown, it is preferable to use the one illustrated in **Figure 6**. Besides the benefit of freeing up more via space this method also has the advantage of keeping the ground path shorter by having the ground side of the capacitor connect directly to one of the device ground pins. This provides a shorter, less inductive ground 'system' around the IC. As frequencies increase, this ground loop area is more critical, so it is a good idea to get into the habit for all designs.

2.6.2.8.7. When there are multiple capacitors of different values assigned to the same supply pin on an IC, you should place the lowest value capacitor closest to the device pin. This is the capacitor that provides switching current for the highest frequency supply current requirement. When the output of a digital device switches from an 'off' state to an 'on' state and vice versa, the current required to do this is quite high for a very brief period of time. If only large value capacitors are available to provide this near-instantaneous current, then due to the longer time constant of these larger capacitors, the output will be unable to switch at the required speed. This can cause serious timing problems in the design. Placing low value capacitors close to the pin helps to supply a small current very quickly to the switching device. This is because of the shorter time constant of these smaller capacitors. Once the output reaches a steady state again the current requirement is reduced.

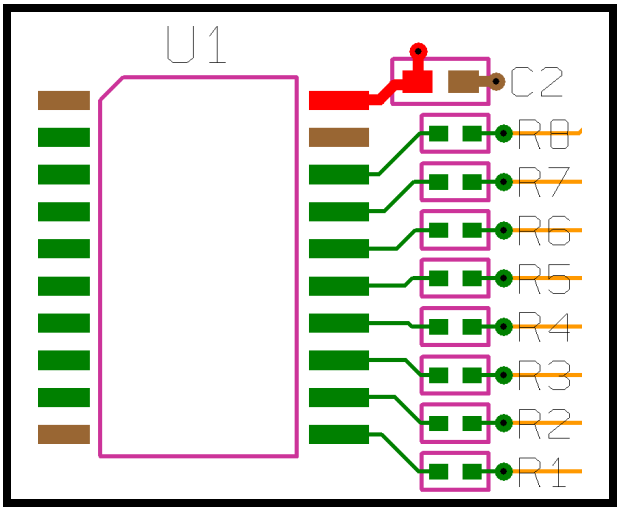


Figure 8: Alternate Routing to Capacitors

2.6.2.8.8. The larger non-polarized capacitors and tantalum capacitors are to be placed near the pin or device in ascending order of value. Tantalums are typically used as an 'area storage tank,' providing the required current faster than could the system power supply. These tantalums recharge the high frequency capacitors more quickly than the system supply can respond.

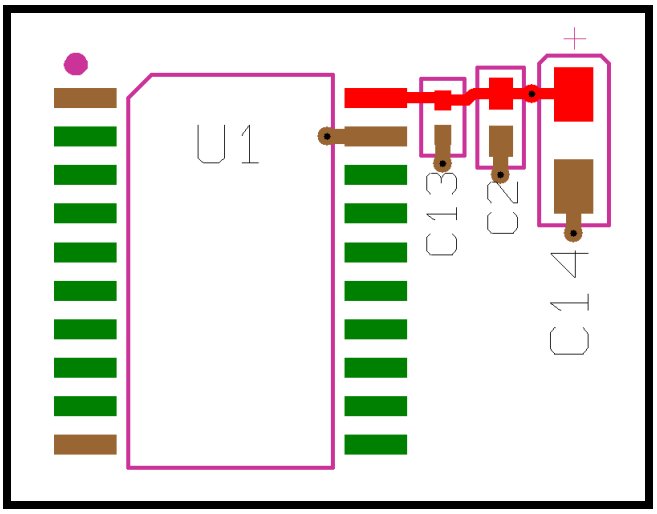


Figure 9: Bypass Capacitors in Ascending Order

2.6.2.8.9. In **Figure 9** the lowest value capacitor, C13 (10nF 0402), is placed closest to the device power pin, followed by C2 (100nF 0603), and finally C14 (10uF 3216). The tantalum could be placed above or below the device without degrading performance, as long as it is close to U1. Usually the space to the left and right of an IC is required for either fanouts or other components that need to be considered before the tantalum. The number of capacitors of each value will usually decrease as the values increase. So there might be four to six ceramic capacitors per tantalum capacitor. Capacitors with values greater than 10uF can usually be dispersed over a larger area.

2.6.2.8.10. Devices with multiple power pins usually need to have at least one bypass capacitor per power pin. Looking at the figures below, if the design only allows for two bypass capacitors on U3, then place one on either side of the device, as in **Figure 10**. However, if this were a 16-bit buffer/driver, it would be particularly susceptible to ground bounce problems, because many outputs can switch simultaneously. If this were the case, then you should make every effort to persuade the engineer to add two more capacitors per device, as shown in **Figure 11**.

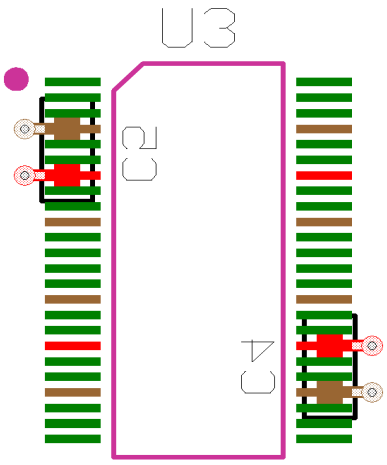


Figure 10: Too Few Bypass Capacitors

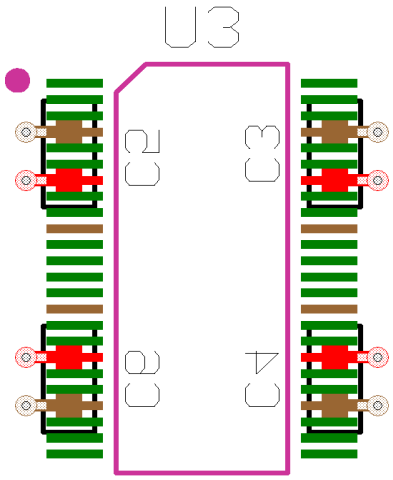


Figure 11: Preferred Number of Bypass Capacitors

2.6.2.8.11. Always refer to the schematic when placing bypass capacitors because there are often logic input pins on digital devices that are 'tied high'. Make sure when placing the bypass capacitors that you are placing them at the device power pins and not at tied high logic pins.

2.6.2.8.12. ***Bypassing BGA packages***

2.6.2.8.12.1. There are a number of methods of bypassing BGA packages, of which the preferred method(s) would vary, depending on the particular BGA pin configuration. The first method shown in **Figure 12** is for a perimeter matrix BGA. This type of package has pins in rows around a vacant center courtyard. It is quite normal for the power and ground pins of these devices to be on the inside rows. This makes it easy to place the bypass capacitors on the opposite side of the board in the courtyard area. Orient the capacitors in such a way that the BGA power pin fanout via can also be the connection point for the capacitor. This gives the lowest inductance path for power and also leaves via space for signal routing.

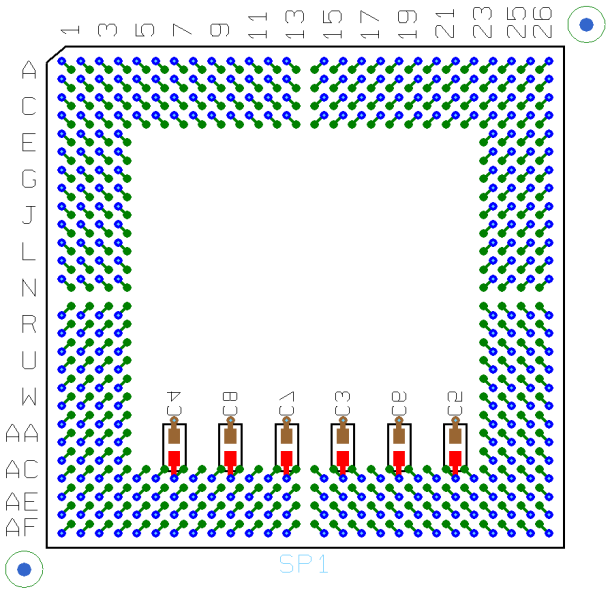


Figure 12: Bypass Capacitors in a Perimeter BGA Courtyard

2.6.2.8.12.2. With solid matrix BGA packages as shown in **Figure 13** and **Figure 14** the bypass capacitors still need to be as close to the device as possible. They can't be close if they are on the top side of the board because there is usually a 0.200-inch component keepout area around a BGA for rework and inspection tools.

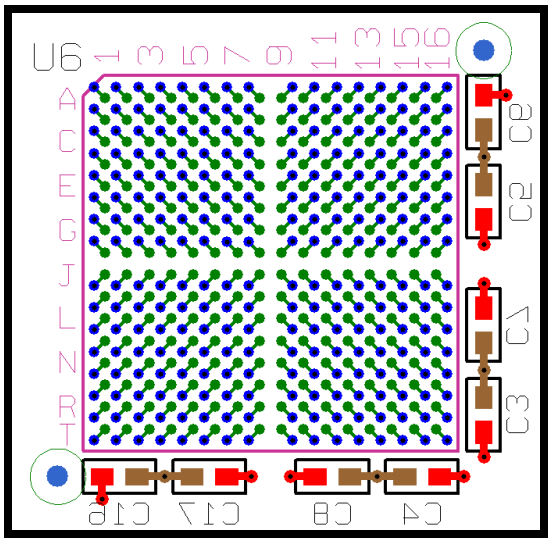


Figure 13: Solid Matrix BGA Bypassing (1)

2.6.2.8.12.3. In order to have them close to the device power pins, they need to be placed on the bottom. Placing some capacitors within the matrix as in **Figure 14** is preferred, if possible, but has the disadvantage that the capacitor pads will show up in an X-ray inspection of the board, and so this method might not be possible. Sharing vias is OK as long as you don't increase the capacitor trace length to do so.

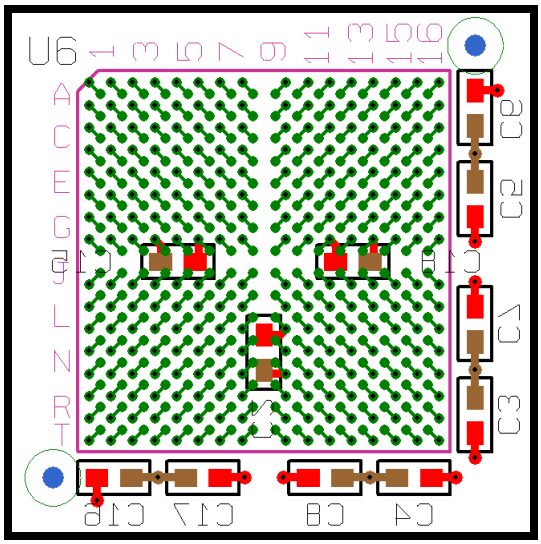


Figure 14: Solid Matrix BGA Bypassing (2)

2.6.2.8.12.4. When placing the bypass capacitors within the matrix, as shown in **Figure 14**, try to do so only when there are existing vias available as part of the BGA fanout pattern. Adding extra vias in these areas is possible. But be aware that extra vias will reduce the wider channels of copper on the internal power and ground planes that are in these areas as a result of the fanout pattern being in four directions.

2.6.2.8.12.5. Capacitors placed as in **Figure 14** often require separate vias for all the connections to power and ground planes. This is usually more of a personal requirement from an engineer. Generally, the more high speed a design is the more this becomes relevant. Sharing vias is often allowed, as in **Figure 12**, and saves routing channels.

2.6.2.8.12.6. These are only general guidelines for bypassing BGA packages. Often you will find that the engineer has a very specific pattern of bypass capacitors that he or she wants to implement for a particular BGA device.

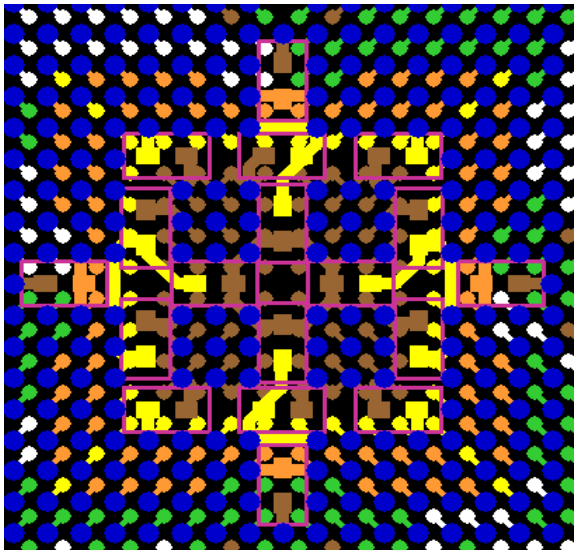


Figure 15: Solid Matrix BGA Bypassing (3)

2.6.2.8.12.7. **Figure 15** shows another useful BGA bypassing technique. There is often a 'solid' block of Ground pins in the middle of a BGA, surrounded by one or two rows of power pins. When this occurs, you can remove the auto fanned-out vias of the outer row of ground pins and fan these pins back in to the next row inside. This technique will provide a channel around the center block of ground pins where you can place bypass capacitors on the bottom side of the board. It may be necessary to reduce the physical size of some of the power capacitors in order to accommodate this. The result is a number of bypass capacitors much closer to the power pins than would have been possible any other way.

2.6.2.8.12.8. The example in **Figure 15** shows eighteen bypass capacitors tightly placed and routed in the middle of a solid matrix BGA.

2.6.2.8.13. ***Bypassing and Filtering of an Integrated RF or Audio Amplifier***

2.6.2.8.13.1. Bypassing and filtering of the power circuit of an integrated RF or Audio amplifier is another very common necessity, and there are some particulars of which to be aware. Consider the following circuit.

2.6.2.8.13.2. **Figure 16** shows a common, single-stage RF amplifier. This may be the only one in a design, but is more commonly one of a chain of amplifiers. This particular device does not appear to have a specific power supply pin, as it uses its output pin (pin 3) as its power supply pin. It is very important to place and route the components around this device in a very specific way. Failure to do so will almost certainly result in poor performance.

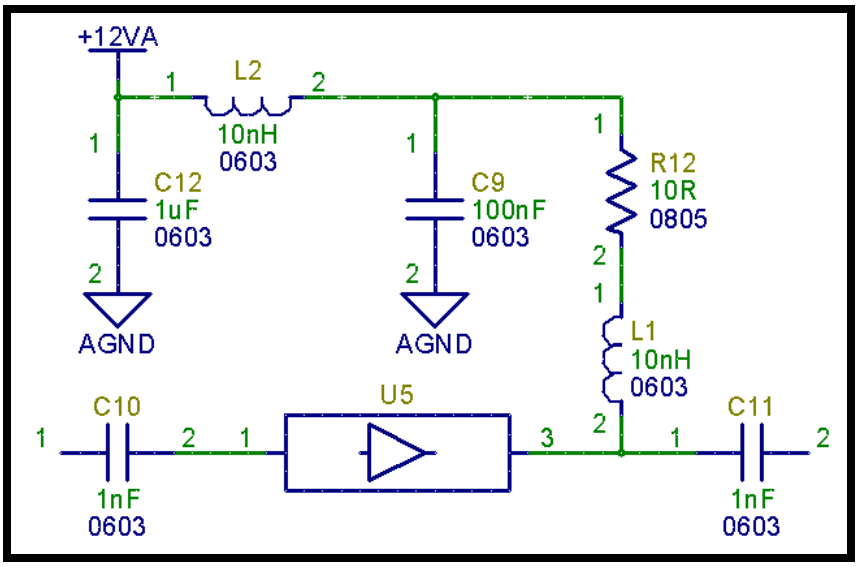


Figure 16: Common RF Amplifier Circuit

2.6.2.8.13.3. An example layout of this circuit can be seen in **Figure 17**. The first thing to be sure of is that the input and output signal paths are kept away from each other. Then we look at how to lay out the power circuitry. The first thing that the power pin should 'see' is the inductor, L1, followed by the coupling capacitor C11. The two bypass capacitors, C9 and C12, should be placed such that their ground end is as close as possible to one of the amplifier's ground pins. Placing the ground side of the capacitors close to the amplifier ground pin keeps the ground circuit loop area to a minimum.

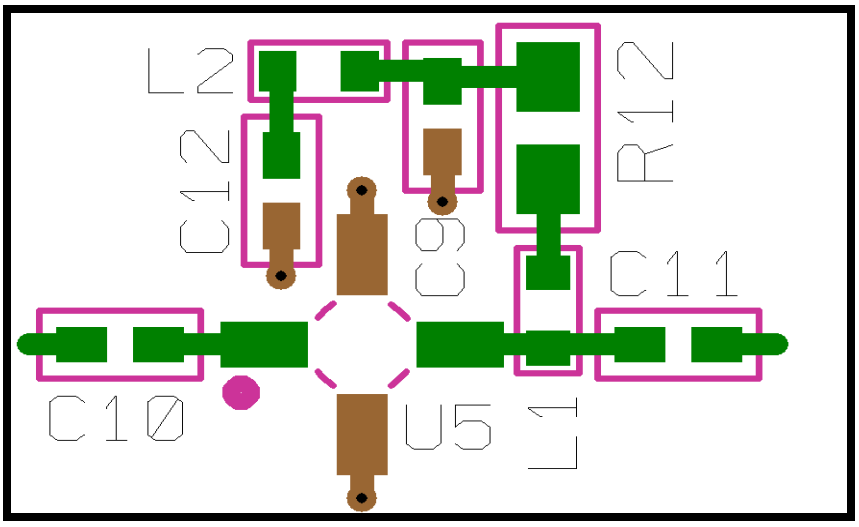


Figure 17: Layout of RF Amplifier Circuit

2.6.2.9. Terminations—Identification and Basic Placement Guide

2.6.2.9.1. It is not always obvious from the way a schematic is drawn just where along a signal path to place terminating devices. It is important for the board designer to know how to identify both the existence and type of terminators

in use. If series and parallel terminators are not placed at the correct end of the line, then they will not function correctly as terminators. This can result in the circuit either not working reliably or even not at all. It is also important to understand under what circumstances termination is required, so that if the design engineer has not implemented it, the board designer can make valid suggestions to change the design. The placement process often reveals an under- or over-use of terminators, at which point the designer should suggest to the engineer the addition of missing terminators or the deletion of existing ones.

2.6.2.9.2. The engineer may include zero-Ohm resistors in the schematic that may eventually become terminators. They start out at zero Ohms because the correct terminating value is not known until post-layout analysis. Zero-Ohm resistors are not used exclusively as unspecified terminators, however. They may also be used as a selector; a placeholder for a range of value options to be selected at assembly time.

2.6.2.9.3. Therefore, it is important to spot the difference between what is intended as a terminator and what may be intended as a selector. In the case of a series terminator, this resistor should be placed as close to the source as practicable. Whereas, in the case of a selector, it makes more sense to place the zero-Ohm resistors close to each other, making their functional use easier to identify. In short, be careful when looking at component values, and do not make assumptions if you are not certain.

2.6.2.9.4. Look at the schematic in **Figure 18**. It is quite common to see a schematic scattered over multiple sheets like this. There is no obvious placement strategy that can be derived from the schematic. Let's work through this and come up with a layout strategy.

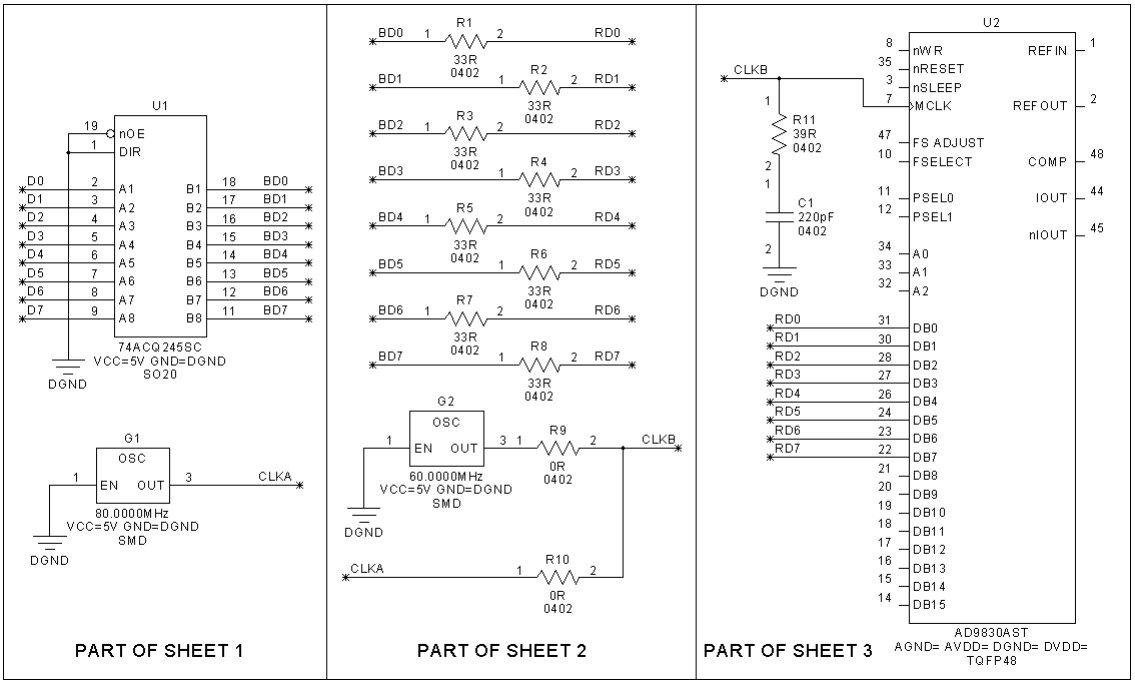


Figure 18: Sample Multiple-Sheet Schematic

2.6.2.9.5. First, we need to determine the function of these components. The main components are:

U1 — a bus driver device
U2 — a digital-to-analog (D-to-A) converter
G1, G2 — two oscillator packs

2.6.2.9.6. These are the components that will determine the overall placement. The bus driver would typically be placed in the area of a processor or other complex digital logic circuit. The two oscillators would possibly also be placed in the digital area, as they may be the source used to derive multiple clocks for the digital circuitry. It is fairly likely, though, that the D-to-A converter would be placed some distance from the other devices, and be in an electrically quieter analog area. This means that the RD[0:7] and CLKB traces to U2 could be long and, therefore, require termination.

2.6.2.9.7. In a digital system, the most commonly used transmission line impedance is 50 Ohms, while the output impedance of most drivers is 20 – 25 Ohms. The data lines from U1 are connected to R1 – R8 on sheet 2 (33 Ohms). If we combine these two values, we get approximately 50 Ohms. By placing these resistors very close to the driver (U1), we make the source impedance of the signal look like 50 Ohms, matching our transmission line impedance.

2.6.2.9.8. Looking at **Figure 19**, notice that the series resistors are placed very close to the driver device output pins. The traces to U2 can be longer because the combined source impedance now matches the line impedance. The ‘output’ side of the resistors now looks like the signal source.

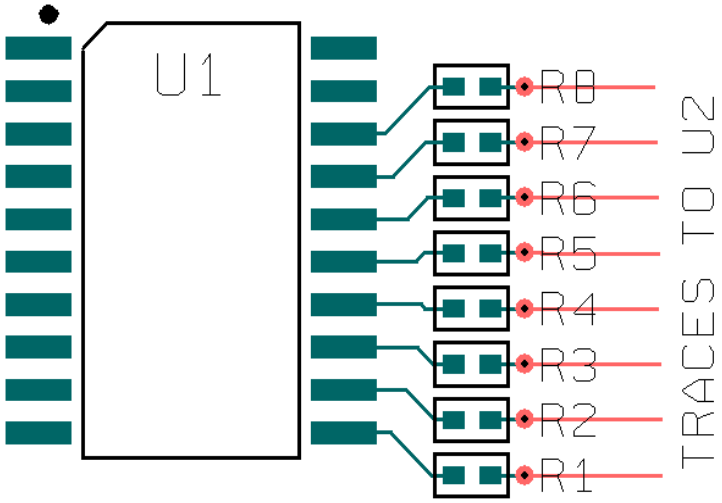


Figure 19: Source Series Terminator Placement

2.6.2.9.9. There is a general rule-of-thumb for series terminators, which states that the terminating resistor should be placed as close as possible to the source pin, and not more than 30% of the total trace length from the source pin.

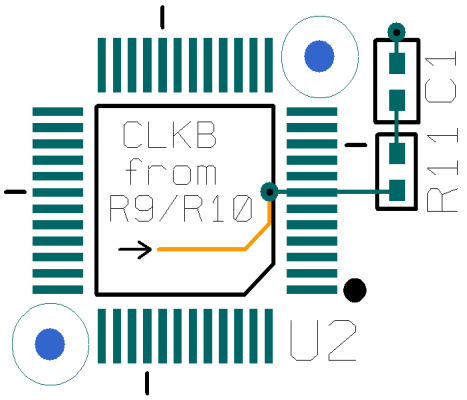


Figure 20: Acceptable Parallel Termination

2.6.2.9.10. Next, we examine the CLKB signal and its termination (**Figure 20** and **Figure 21**). In this case the terminator is a parallel R/C type made up of R11 and C1. The combination of the 39-Ohm resistor and the impedance of the 220pF capacitor at the frequency of concern are designed to be approximately 50 Ohms. This matches the characteristic impedance of the trace and, therefore, provides ideal termination. The actual values will vary (mainly the capacitor value), depending on the frequency of the signal being terminated, but these are typical values.

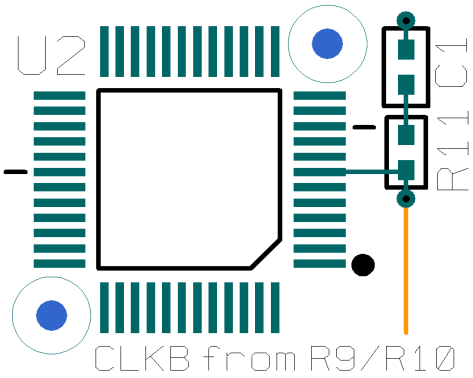


Figure 21: Best Parallel Termination

2.6.2.9.11. Notice in **Figure 21** that the signal from the oscillators goes first to the terminator and then on to the pin of U2. This is usually acceptable, but ideally the signal should go to U2 first and then to the terminator, as in **Figure 20**. This way U2 is on a terminated portion of the trace instead of a short stub. In very high frequency designs (>300MHz), even this short stub can cause serious problems.

2.6.2.9.12. The last consideration in the layout of the schematic of **Figure 18** is the CLKB frequency selection resistors (R9 and R10). One of these will be loaded at the assembly stage, but the other will not. If they are placed at the D-to-A (U2) end of the CLKB signal, then the output of both oscillators will have to be routed the full distance from the oscillators to the D-to-A. If the resistors are placed at the oscillators' end, then the two traces from the oscillators are very short, and only one trace (CLKB) needs to travel the distance to U2.

2.6.2.9.13. We must also consider the issue of noise emissions from the board. In the case of placing the resistors at the D-to-A end (and only loading one resistor), the trace to the pad of the non-existent resistor has the potential of acting as an antenna, possibly causing some serious electro-mechanical interference (EMI). This effect will be dependant on the frequency of the signal, and the length and topology of the trace. This trace should be routed on an inner layer, but if it is accidentally routed on an outer layer, then the EMI problem can be much worse. Now let's examine our options for the physical layout.

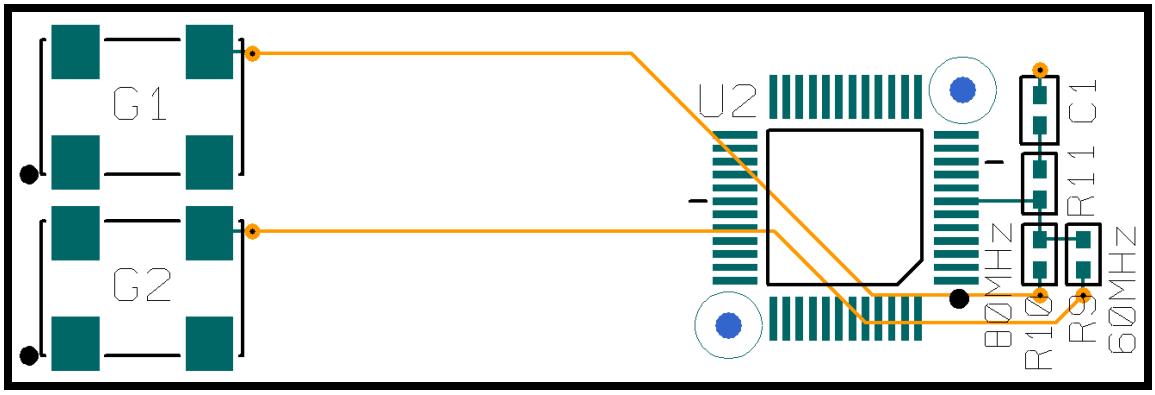


Figure 22: Clock Select Resistors -- Poor Placement

2.6.2.9.14. Notice in **Figure 22** that the resistors are at the D-to-A end. Oscillators G1 and G2 might be a considerable distance away, and we have to route both output traces the full distance. This is not a good design as a result of the poor placement of resistors R9 and R10.

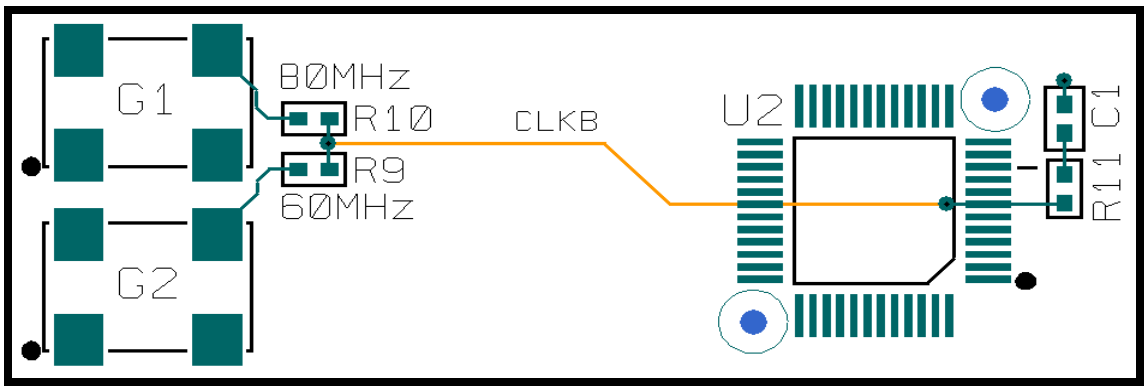


Figure 23: Clock Select Resistors -- Good Placement

2.6.2.9.15. In **Figure 23**, the resistors are at the oscillators' end. We only need to route one trace, which is not an antenna because it is always terminated. The trace from the oscillator to the non-existent resistor is not likely to act as an antenna because it is very short, unless the frequencies are extremely high (towards or above the 1GHz range).

2.6.2.9.16. It is also quite common to have to tune a clock trace length to match the length of other clocks or data signals in the system. In this case the layout in **Figure 23** is better, again, because only one trace needs to be tuned, requiring probably only half the tuning space that would be required if the layout shown in **Figure 22** was used.

2.6.2.9.17. Lastly, since most engineers like to specify larger clearances to clock traces, there would be fewer available route channels on the clock layers if the layout of **Figure 22** was to be used because of the existence of the two long, tuned clocks instead of just one as in **Figure 23**.

2.6.2.10. Mixed Analog/Digital

2.6.2.10.1. Placement of mixed analog/digital circuits is critical in order for the combined circuit to function correctly and to avoid any possibility of the different sections of the board interfering with each other.

2.6.2.10.2. These types of designs usually have quite clearly defined analog and digital sections, with only a few connections in common. The power and ground systems are usually separated, with the ground systems being connected somewhere close to the area where the common signals are connected. If A-to-D or D-to-A converters are used, these devices normally have analog signals on one side of the device and digital signals on the other side. This usually makes it quite easy to place the different circuits so that analog signals are not routed in digital areas and vice versa. Another thing to remember is that the A-to-D or D-to-A device should always be placed close to the beginning or the end of the analog area. This gives the shortest possible trace length for the analog signals. Even when there are many more digital traces than analog (up to 20:1), it is still much better to place the converter device right at the analog circuitry.

2.6.2.10.3. Because the analog and digital signals are usually in different areas on mixed technology devices, it is usually quite easy to identify where to place a split in the ground planes. Proper circuit placement and, if necessary, the addition of route obstructs, will ensure that no signal traces of one technology are routed over areas of another technology.

2.6.2.10.4. There should normally be a point between the different circuit areas where the ground systems are tied together (a 'bridge'). The designer should analyze how many traces connect between the different circuits and allocate these evenly over the available routing layers. Then, using the required impedance and spacing parameters, decide how wide to make the bridge that connects the ground systems such that all signals between the different circuit areas are routed over this bridge. This will ensure that all these signals have a tightly coupled return current path.

2.6.2.11. Analog and RF designs

2.6.2.11.1. An analog circuit should be placed much as it is drawn on the schematic. However, there are a number of things to be aware of when placing analog circuits. Often analog devices will have two or three bypass capacitors for each supply. These must be placed as close to the device power pins as possible. Always place the lowest capacitance value closest to the pin and the highest value furthest from the pins.

2.6.2.11.2. Try to orient these components in such a way that the ground side of the capacitors is as close to the device ground pins as possible, as this reduces the ground loop area for the device.

2.6.2.11.3. Be sure when you are placing circuits like this that you do **not** place inductors parallel and adjacent to each other, as doing so will most likely cause mutual inductance problems. Placing inductors at 90-degree rotations is best because their magnetic fields are then perpendicular, and there is minimal mutual inductance.

2.6.2.11.4. It is more important that analog circuits be placed for optimal functionality, and this is often not the 'neatest' looking solution. You need to be aware of the signal path, and then to place the components in order to optimize this path. If the signal path is not apparent from the way in which the schematic has been drawn, then ask the engineer for clarification, and then highlight the schematic to show the signal path.

2.6.2.11.5. Analog circuits are often comprised of long paths of components placed in a signal path flow. There is often a need to 'wrap' these circuits around in order to fit them in the available space. When this is done, it is important to try to maintain maximum distance between input and output parts of the circuit. One way of doing this is to keep the 'signal path' components in a line around the outside of the circuit and have all the ground areas in the middle.

2.6.2.11.6. Once placed, an analog design has little need to consider how to route it. Analog and RF designs are usually 95% placement and 5% routing, so the signals are nearly always extremely short and point-to-point.

2.6.2.12. Thermal Considerations

2.6.2.12.1. All parts will generate heat whenever a current flows through them, although most parts only create a moderate amount of heat. Some parts, however, are considered heat generators, while others are heat sensitive, both of which require special thermal considerations.

2.6.2.12.2. If heat generators are present in a design, then they must be cooled appropriately. This may involve heat absorption material ("heat sinks") or placement in a special high volume air channel within the box. Examples of heat-generating parts are power supply components and high pin count or high-speed devices.

2.6.2.12.3. If heat sensitive parts are also present, then they must be located away from heat generators, or be cooled appropriately, if they must be placed close by. Crystals and oscillators are both examples of devices that are sensitive to heat. The designer needs to be aware of all components' heat requirements, and the methods that the electrical and mechanical engineers want to implement in order to meet these requirements.

2.6.2.12.4. This concludes our discussion of Electrical Placement. We continue with a discussion of Manufacturing Placement issues.

2.6.3. Placement: Manufacturing

2.6.3.1. The second element to a successful placement is that it meets Manufacturing's physical assembly requirements. Prior to starting a design, the designer must know how many boards are intended to be made: High Volume, Mid/Low Volume, or Prototype only. Typically at ODA, designers are to layout all boards for high volume manufacturing, but if it is clear from the very beginning that the boards are very low volume, or will only be made for prototype purposes, then the designer will be allowed a bit more flexibility in how a board is placed. Designers are to make appropriate decisions based on the manufacturing needs on the client. Remember:

2.6.3.1.1. **Design decisions are evaluated in light of their effect on the processes that follow it—Fabrication, Assembly and Test.** *(The ODA Mission Statement)*

4.1.1.1 Part-To-Board-Edge Clearances

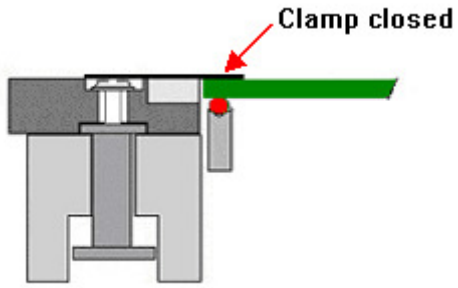


Figure 24: Clamp Closed

2.6.3.2. In order to automate any portion of the board assembly process, stuffed cards must be able to travel on a conveyor transport system. As a general rule, top side components must be clear from the two long sides of the board outline by .120" (3mm) and .200" (5mm) on the bottom side. If this condition can't be met, then the designer must add either 1 or 2 rails as necessary (see Breakaway Rails in Mechanical Section). **Figure 24** and **Figure 25** illustrate two possible types of conveyor transports: Clamp closed and Edge clamp open.

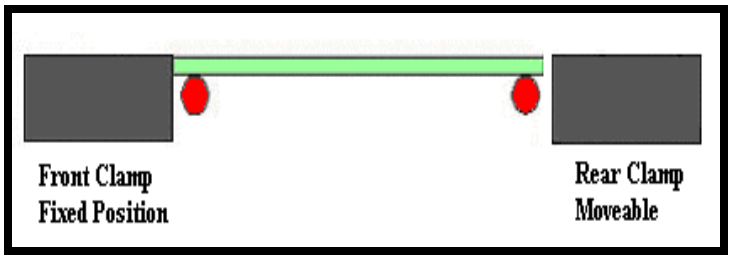


Figure 25: Edge Clamp Open

2.6.3.3. Part-To-Part Clearances

2.6.3.3.1. The most common difficulty encountered by the assembly house is a component placed too closely to another component. When the designer places components too closely to one another, it creates a myriad of problems with pick & place equipment, soldering equipment, inspection, and rework. In order to avoid these problems, never place components closer than the minimum allowable component spacing.

2.6.3.3.2. The minimum component spacing depends upon the type of devices that are located next to each other. APPENDIX F: ODA Part to Part Clearance Matrix (Section III, page 112) specifies the minimum spacing between various components. Designers must place components according to this matrix, unless the client dictates otherwise. However, you should remember that this matrix represents the closest that parts may be placed, and to always maximize the space between components.

*2.6.3.3.3. **Shadowing***

2.6.3.3.3.1. When adjacent components have great differences in height, “shadowing” may occur, in which the tall component blocks the short component from heat during the soldering process or cooling during normal operation. The designer must take steps to reduce the amount of shadowing that occurs in a design. **Figure 26A** shows the possible problems during the soldering operation when low-profile components are placed too near high-profile parts. Half of the connections on the surface-mount component could have cold solder joints, causing short- and long-term problems.

2.6.3.3.3.2. **Figure 26B** shows good and bad placement of high-wattage components. Avoid placing such parts behind high-profile components. Being “behind” is determined by the direction of air flow over the board surface when it is put into its final assembly package.

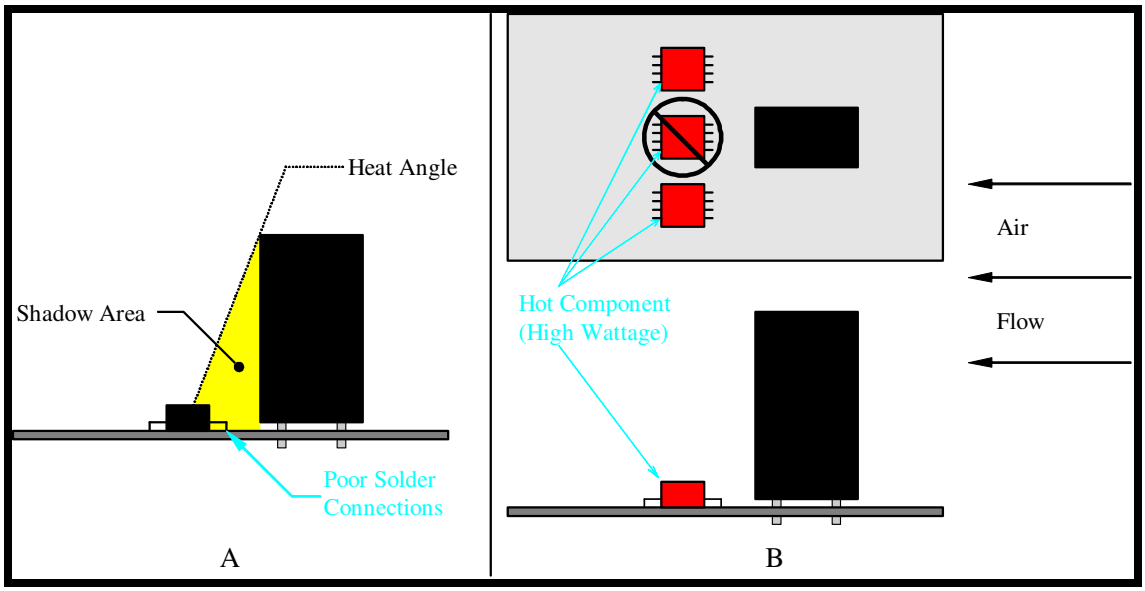


Figure 26: Part Location Around Tall Components

2.6.3.3.4. ***Selective Wave***

2.6.3.3.4.1. For double-sided, surface-mounted assemblies containing bottom-mounted QFPs, BGAs, small discretes less than 0603, and fine pitch SOs (that is, .65mm pin pitch or less) and that also contain enough thru-hole components to make wave soldering practical, a selective wave solder fixture will be needed (see **Figure 27**).

2.6.3.3.4.2. In order to reduce the number of open areas in a selective wave fixture (thus reducing tooling costs), try to segregate thru-hole components from SMT components larger than SOIC16 in different areas of the board. The larger the open area around a thru-hole the better, since a larger area allows for better solder flow. It is also extremely important to keep a .150" minimum (.250" preferred) clearance from an SMT body to a thru-hole component pin. Allowable wave components can be closer to thru-holes (per ODA standards) as long as they can be included within an open area, and allow for a wall or closed area to be built around them with a .250" clearance to other components outside the open area.

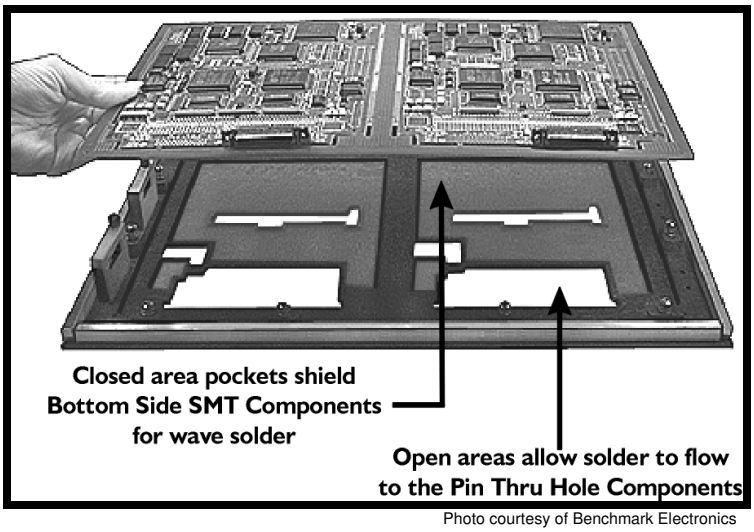


Photo courtesy of Benchmark Electronics

Figure 27: Selective Wave Solder Fixture

2.6.3.4. Orientation

2.6.3.4.1. The two aspects of component orientation are:

2.6.3.4.2. To keep like-component rotations to a minimum (ODA preference would be no more than two rotations) and,

2.6.3.4.3. For bottom side components needing to be wave soldered, to orient components optimally according to how the board will enter the wave solder machine (see **Figure 28**).

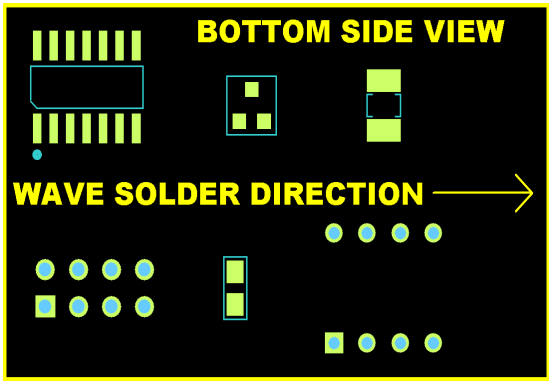


Figure 28: Component Orientation for Bottom Wave Solder Process

2.6.3.5. Bottom-Side Components

2.6.3.5.1. When 'real estate' limitations or electrical constraints require mounting SMT components on the bottom side of the board, the designer must weigh performance issues against process issues. Before determining which components to allow on the bottom, the designer must first determine which soldering process will be used: reflow/reflow (double reflow), double reflow/selective wave, or reflow/wave. Use the chart below to determine which components to allow on the bottom.

Table 1: Part Placement Chart

Component Type	Double Reflow	Double Reflow/ Selective Wave	Reflow/ Wave
Thru-Hole			
J-Lead			
Chip	✓	✓[1]	✓[2]
Gull Wing	✓	✓[1]	✓[2]
Gull Wing(<.050" pitch)	✓	✓	
Leadless	✓	✓[1]	
Plastic BGA	✓	✓	
Ceramic BGA			

✓= approved bottom mount
[1]height not to exceed .175"
[2]thermally rated for wave

2.6.4. ODA Project Checklist (Placement Section)

2.6.4.1. At this point all Placement items within the ODA Project Checklist spreadsheet should be marked off (marked off means done or considered).

2.7. ROUTING

2.7.1. At this point in the layout process, for the most part, the engineer has approved the placement, and the design is ready for routing. This is the point at which many designers get a bit impatient and just start routing traces without setting up the proper route parameters. Of course, this likely results in a poor design and the re-doing of work. From the pre-layout interview, reviewing of provided routing data (application notes and customer guidelines), and on-going communication with the engineer up to this point, it is imperative that the designer have formulated a route strategy before one trace is routed.

2.7.2. Below is the typical ODA process for routing a board:

2.7.2.1.	**Routing Parameters Data Entry**	Enter data—such as layer stack-up, trace widths (impedance), via type, net ordering, pairs, and signal timing—into the appropriate tool set.
2.7.2.2.	**Pin/Gate Swapping Data Entry**	If allowed by the engineer, pins and gates of a device are to be swapped to improve routing. Perform this step after Process #3, Fanout, if preferred.
2.7.2.3.	**Fanout**	All SMD devices are to be fanned-out for internal trace routing, as well as creating placeholders for ICT.
2.7.2.4.	**ICT Review**	Review in-circuit test point placement for probability of percentage of coverage.
2.7.2.5.	**Plane Shapes Entry**	Draw in any plane shapes of different voltages on the appropriate power or signal layers.
2.7.2.6.	**Critical/Interactive Routing**	Analog circuitry, off-board interface connections, very short routes, and regular patterns flows (memory areas) should all be hand routed.
2.7.2.7.	**Critical Route Review**	This is a good point (i.e., after critical routes are done, but before routing is complete) to send the database to the engineer for review.
2.7.2.8.	**General Routing**	If appropriate, use the auto-router to route the rest of the open nets; otherwise, hand route the remainder of the board.
2.7.2.9.	**Clean-up and Review**	Make a visual scan of each layer to ensure cleanliness as well as manufacturability of the routes. In addition, review appropriate reports to be sure the routes have met all of the rules provided by the engineer.
2.7.2.10.	**In-Circuit Test Placement**	If required by the engineer in the pre-layout interview, place ICT probe points per ODA standards.
2.7.2.11.	**Plane Shapes Processing**	Once all the routes are complete and clean, the plane shapes must be processed and reviewed.
2.7.2.12.	**DRC/Review**	Run a full Design Rule Check (DRC), and send the design to the engineer for a final route review.

2.7.3. Routing Parameters

2.7.3.1. Many of today's designs have a very high percentage of nets that have some type of routing constraint. For this reason, it is very important to enter these routing parameters into the EDA tool to ensure that all the rules are met. This section will discuss the following common routing parameters: Layer Stack-up, Net Groupings, Net Ordering, Impedances, Vias, Pairs, and Net Timing.

2.7.3.2. Layer Stack-Up

2.7.3.2.1. PCB layer stack-up can play a major role in the success or failure of a design. This becomes more significant in higher speed designs. There are some basic rules to observe.

*2.7.3.2.2. **Keep it Balanced***

2.7.3.2.2.1. Always keep the stack-up as 'balanced' as possible. That is, distribute planes and signal layers symmetrically about the Z axis

center of the board. This is done to prevent board warpage caused by different material thicknesses from one side of the Z axis center to the other.

2.7.3.2.2.2. Copper weights should also be balanced about the Z axis center, and for the same reason, namely, to reduce board warpage. If it is necessary to have higher copper density on one side of the Z axis than the other by having, say, an extra plane on one side, then let the fabrication house know that they can add copper hatching in free areas on the internal layers. They will then add hatched areas in the free space on signal layers to try to balance the copper about the Z axis.

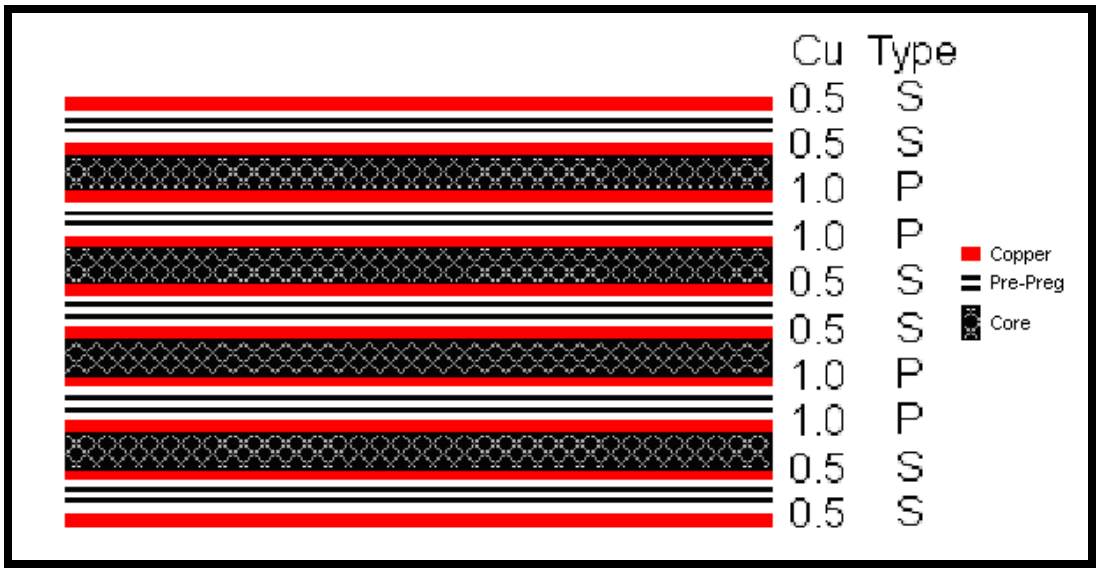
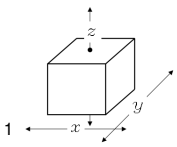


Figure 29: Symmetrical Ten-Layer Stack-up

2.7.3.2.2.3. **Figure 29** shows a perfectly acceptable ten-layer stack-up. It is symmetrical about the Z axis[1] center, and it also meets the requirement of balanced copper weights. Fabrication houses can provide copper cores with the same copper weights on each side, but can also provide cores with different copper weights, as specified in this example stack-up.

2.7.3.2.2.4. The stack-up shown above is fine for the majority of applications, but you need to be aware that there are circumstances where more careful consideration needs to be given to the usage of cores, and that such situations are becoming more prevalent. Notice that the two sets of power plane layers (3|4 and 7|8) are separated by a layer of pre-preg rather than core material. This type of layer assignment prevents the use of buried capacitance cores for the power and ground plane pairs, which may be essential to achieve, given a design's particular board performance requirements. The following figures show some

1 

alternative stack-ups that will provide buried capacitance cores for the same ten-layer board.

2.7.3.2.2.5. The first alternative is to use cap lamination as the process for the outer layers (see **Figure 30**). This gives the desired result, in that the power and ground planes now share the same cores and can therefore now be made using buried capacitance cores. This is usually required for high speed designs. The disadvantage of this stack-up is that most manufacturers prefer not to cap laminate.

2.7.3.2.2.6. The second alternative (see **Figure 31**) is to use a single sided core for layers 2 and 9 and then foil laminate for the outer layers. This still gives us balanced cores and copper through the Z axis, and keeps the power and ground planes on the same cores.

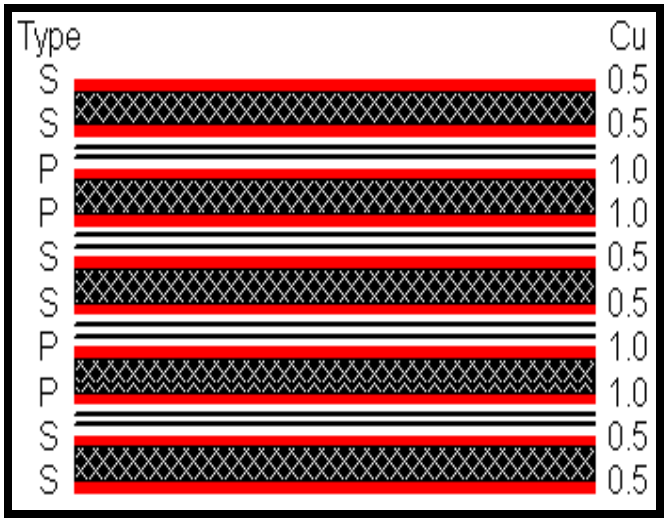


Figure 30: Cap Lamination Stack-Up

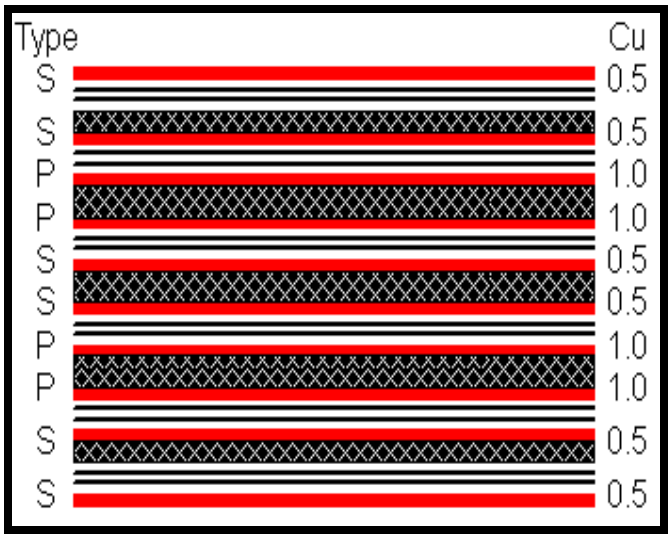


Figure 31: Single-Sided Core Stack-up

2.7.3.2.3. ***Low Speed Designs—Power/Ground Planes can be separated***

2.7.3.2.3.1. It is preferred to keep power and ground plane pairs on adjacent layers. However, in low-speed designs, power and ground planes may have signal layers sandwiched between them, because the return currents of low-speed signals tend to follow the path of least resistance instead of the path of least inductance. However, before separating the power and ground planes, make certain the board you are working on is, in fact, a low-speed design[2], which may not be readily apparent. Because of the difficulties in determining the speed of a design, it is a good practice to completely avoid splitting the power and ground plane pairs.

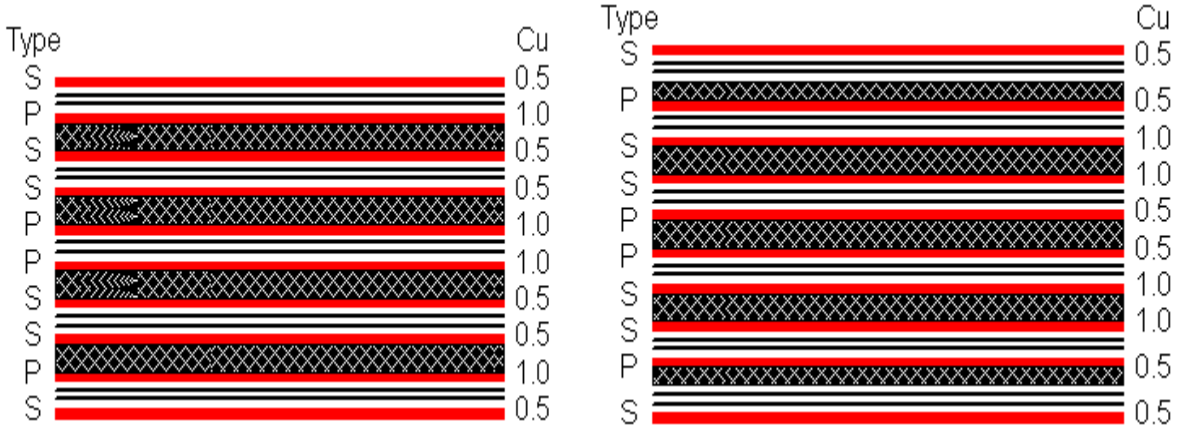


Figure 32: Balanced Stack-Up with Separated Planes

2.7.3.2.3.2. **Figure 32** shows two alternatives for creating separated planes in a balanced stack-up. The first has the adjacent planes on layers 5 and 6 as sharing cores with signals on layers 4 and 7, while the second shows the same layer usage, but with the middle power planes on the same core. In a design where only one power plane is required, this is quite a good solution because both the planes on layers 2 and 9 can be ground planes and, therefore, provide extremely good environments for all the internal signal layers.

2.7.3.2.3.3. Please note that, while layers 4 and 7 are allocated as signal routing layers in this stack-up, you will need to be selective about which signals to route on the layer that is next to the power plane. This is because power planes are usually noisier than ground planes. You should avoid routing highly sensitive traces (such as clocks or low level analog signals) on the layer adjacent to power.

2.7.3.2.3.4. Choose between these and the previous stack-ups based on the number of power planes required. If you need multiple power planes, it is best to keep them paired with a ground, as shown previously. However, in these ten-layer examples, this means having two signal layers at the top and bottom of the stack. Many engineers will prefer to keep layers 2 and 9[3] as ground planes to help minimize electro-

[2] Low speed is not determined by the board's clock frequency (which is a common misconception among designers), but rather by the edge rate of the components. The edge rate is the rise time and fall time of the signals generated by the device, which are independent of the fundamental frequency at which the device is running. Many formerly low-speed devices have been remanufactured with lower rise and fall times, which means that there are fewer and fewer 'low speed' designs any more, since most current designs, even at lower fundamental frequencies, are still using high edge rate devices.

[3] Or, more generally, *n*-1, the layer next to the bottom layer.

mechanical interference (EMI) from the board. The stack-ups that follow are better suited to designs with only one power plane required. If there is any ambiguity as to which way to go, make sure to discuss the issue with the engineers on the project, since they may have requirements that you have not considered.

2.7.3.2.4. ***High Speed Designs—Keep Power/Ground planes together***

2.7.3.2.4.1. In high speed designs it is imperative that the power/ground plane pairs are not separated. This is because a high speed signal return current will follow the path of least inductance. This is always going to be in the closest plane to the signal. In many cases this return signal will flow in the power plane, and not in the ground plane. However, the return current must at some point find a way to the ground plane. If the planes are close together, then the highest frequency harmonics content of the return signal may find its way to the ground system by way of the planar capacitance between the two planes. This is advantageous because these harmonics are a significant contributor to EMI.

2.7.3.2.4.2. As the planes are separated, the only path left for a high speed return signal to get to ground is by way of the bypass capacitors that are distributed around the board. In many cases these capacitors are not of a low enough value to provide low enough impedance at the highest harmonic frequencies. Higher impedance will cause a voltage to be generated across the capacitors and this will contribute to EMI. The planar capacitance between closely coupled power and ground planes is generally of much lower value than the bypass capacitors. It is often beneficial to have some low value capacitors sprinkled around the board to help with transitioning return currents from power planes to ground planes.

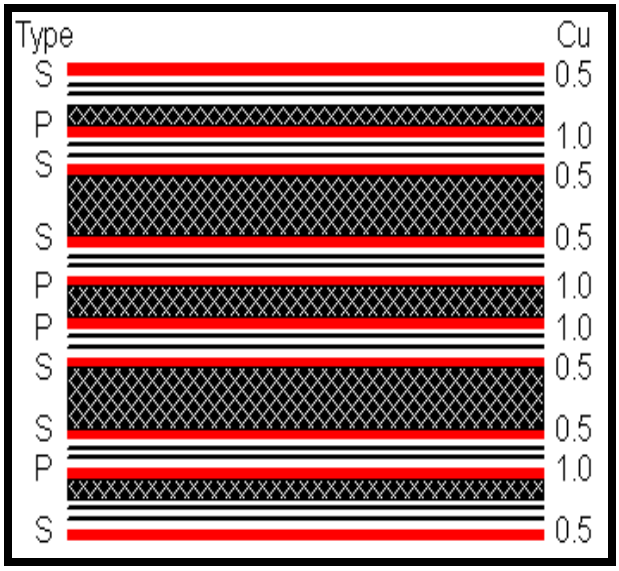


Figure 33: Variation in Core Thickness

2.7.3.2.5. ***Core Thicknesses***

2.7.3.2.5.1. In these designs it is also worth considering core thicknesses and their usage. Make sure to use thin cores for power plane pairs,

and then use thicker cores where possible for signal layer pairs. This means that signal layers will be further apart from each other and closer to their adjacent power or ground planes, resulting in less coupling between signal layers for reduced crosstalk, and tighter coupling between signals and planes for improved impedance control. Impedance shadowing is also reduced because the adjacent shadowing signal is farther away and the closest layer to a signal has by far the greatest affect on impedance.

2.7.3.2.5.2. Notice how the stack-up in **Figure 33** shows increased thickness between the signal layers and reduced thickness between the power plane pairs. This is an almost ideal stack-up to achieve both ease of manufacturing and high signal integrity. In this arrangement, signals are very tightly coupled with the adjacent planes, giving good controlled impedance and, at the same time, the signals are well distanced from the adjacent signals for reduced crosstalk.

2.7.3.2.5.3. The only area in which this stack-up may be limited is on the modeling for differential pairs. As signal layers get closer to their adjacent power layer, a thinner and thinner trace width is required, in order to maintain a given impedance. At a certain distance, the required trace width becomes too small to be manufactured. Be sure to check with either the project engineers or the manufacturer for the availability of the required impedance models.

2.7.3.2.6. ***Only two signal layers at a time***

2.7.3.2.6.1. Never stack more than two signal layers adjacent to each other. If all signal layers are immediately alongside power or ground planes, then they are as close as they can be to their high speed return paths. Stacking more than two signal layers together means that the inner layers of the group are separated from their return paths, which increases the loop inductance of these isolated signals and results in significantly increased EMI.

2.7.3.2.7. ***Orthogonal Routing and Parallelism***

2.7.3.2.7.1. Always route adjacent signal layers orthogonally. Routing in the same direction on adjacent layers will cause crosstalk problems. Of course, when routing high density designs, it is impossible to avoid signals on adjacent layers routing over each other for short distances. However, biasing adjacent layers orthogonally will keep this to a minimum. Crosstalk is not just a function of parallelism; it is more a function of length of parallelism. Signals routed over each other on adjacent layers to escape a BGA, for example, are not likely to cause significant crosstalk.

2.7.3.2.7.2. You need to be careful which signals you allow to route over each other on adjacent layers. Another thing this causes is ‘shadowing’. When this occurs, the characteristic impedance of the signals will change because the reference to the plane is different. For critical controlled impedance traces, shadowing should be avoided.

2.7.3.2.8. ***Split power planes***

2.7.3.2.8.1. With the complex power requirements of today’s devices combined with their high-speed characteristics, the need to supply split power planes is becoming both more common and significantly more

difficult. Beside the standard two power connections (PWR and GND), many devices require one or more additional voltages. For instance, Ball Grid Arrays (BGAs) often require four or more supply voltages. These additional voltages are often local to the device, so we don't want to dedicate an entire layer to them. The result of this is split planes with many local voltage islands on them. This is also true of designs with multiple ground systems.

2.7.3.2.8.2. Since we know that a high speed signal return current may be flowing in these plane islands, or a high speed, controlled impedance signal trace itself may be on an adjacent layer, how do we avoid interrupting the return path, or changing the trace impedance, when the signals cross the splits between the planes? There are several methods to accomplish this goal. The first method is to make sure there is no routing on layers adjacent to the split planes. This can be done by sandwiching the split power planes between two solid ground planes using a GND↔PWR↔PWR↔GND layer stack-up, probably in the Z axis center of the board. One or both of these power planes can now be split without having any effect on signal quality.

2.7.3.2.8.3. A second method is to put the split planes on layers 2 and *n*-1, and then have a solid ground plane on layers 3 and *n*-2. This also works well, but you need to be careful with fanout traces for high speed signals. Make sure the fanouts on layers 1 and *n* do not cross over the splits in the planes on layers 2 and *n*-1. It is also a good idea, if this technique is used, to place surface layer ground plane shapes under critical components like oscillators, to prevent any possibility of noise on the power planes coupling into sensitive components on the surface.

2.7.3.2.8.4. A third method is to place route obstructs, coincident with the plane splits, on the adjacent signal routing layers. This will prevent any routing from crossing the splits. This method is more time consuming and is not the recommended way to do the job. It also means that if an ECO causes a change in the planes shapes, then the adjacent layer obstructs will have to be edited as well. However, on some designs, this may be the only alternative. If this method is used, it is imperative that it be noted in the designer's notes section of the project checklist for reference by other designers who may work on the design in the future.

2.7.3.2.9. ***Signal Transitioning***

2.7.3.2.9.1. Signals that are routed on layers alongside power should ideally not transition to layers alongside a different power plane. Obviously this can't be completely avoided in high density designs, but make sure that at least the critical signals are routed according to this guideline. This will usually be accomplished through the use of manual routing, since the CAD tools do not yet give us the control over these parameters.

2.7.3.2.9.2. When a signal routed on a layer next to power needs to transition to another layer, make sure it is to a layer alongside a ground, and also make sure there are one or more ground vias close to the transition point and, ideally, a high frequency bypass capacitor nearby. If the signal transitions to a layer alongside a different power plane, then it is possible that we could induce noise from that power supply into the return signal.

2.7.3.2.10. ***Clocks and other critical traces***

2.7.3.2.10.1. Clocks and other critical high speed traces should be routed on layer pairs that are between two solid ground planes, if possible. This will provide the least noisy environment for these signals.

2.7.3.2.11. ***Crosstalk Prevention***

2.7.3.2.11.1. When determining the stack-up, make sure to minimize the distance between adjacent power and ground planes, minimize the distance between a signal layer and its closest plane layer, and increase the distance between adjacent signal layers a little. This will give maximum coplanar capacitance, maximum coupling between a signal and its reference plane for low impedance return paths, and maximum distance between signal layers to reduce both crosstalk and impedance shadowing.

2.7.3.3. Net Grouping (Net Classing)

2.7.3.3.1. Net grouping (or net classing) is helpful to organize the routing of a design. Net grouping helps control nets in smaller, more manageable sections. Net grouping should not be confused with Net Ordering or Timing Constraints, which are routing parameters discussed in following sections.

2.7.3.3.2. Even though net grouping is a function that is resolved by the designer, and can be defined in any way the designer wishes, using too many classes can make the design cumbersome. It is the preference of many that classes are organized in a fashion that is more precise and, therefore, better to cluster nets that share common physical factors, instead of common logical factors. Some example physical factors are:

2.7.3.3.2.1.	**Layers to route**	Which layers of the design that specific classes are allowed to route and not allowed to route
2.7.3.3.2.2.	**Via stack**	Which Via stack a specific class is allowed to utilize; Also keep in mind this would include which Via span is allowed
2.7.3.3.2.3.	**Trace width(s)**	For any class, impedance should be considered. Therefore, inputting a modeled trace width for a given layer will ensure that impedance control can be maintained.
2.7.3.3.2.4.	**Trace width range**	Minimum and maximum width allowed within a group; Or if no range desired, the smallest width allowed (projected by board technology) must be specified for the design
2.7.3.3.2.5.	**Spacing of traces within a pair**	When a class is destined to be a controlled impedance pair, a modeled width and spacing is considered.

2.7.3.4. Clearance rules can now be created. By using classes with other classes, we can now set rules to which our tools will adhere while we are designing.

2.7.3.5. A standard matrix example of Net Class groups may be as follows:

Table 2: Example Net Class Groups

	Layers to route	Via	Widths	Pair Spacing	Special Considerations
Power	Specify layers	Specify Size	Specify Min/Max		Nets Which will be routed
Plane	Specify layers	Specify Size	Specify Min/Max		
Clock	Specify layers		Specify Imp. width		Usually requires special spacing
BusHS	Specify layers		Specify Imp. width		Usually requires special spacing
Pair_110	Specify layers		Specify Imp. width	Specify Pair Gap	Usually requires special spacing
(Default)	Specify layers		Board Technology		

2.7.3.6. Trace Widths / Impedance Requirements

2.7.3.6.1. Designs where signal integrity is of the utmost importance require extra attention. One way to control signals is to match transmission impedance. Impedance is a critical requirement because a transmission line with unbalanced impedance could exhibit reflections, which result in two types of distortion:

- Overshoot: a type of reflection, which adds amplitude to the original signal
- Undershoot: a type of reflection, which subtracts amplitude from the original signal

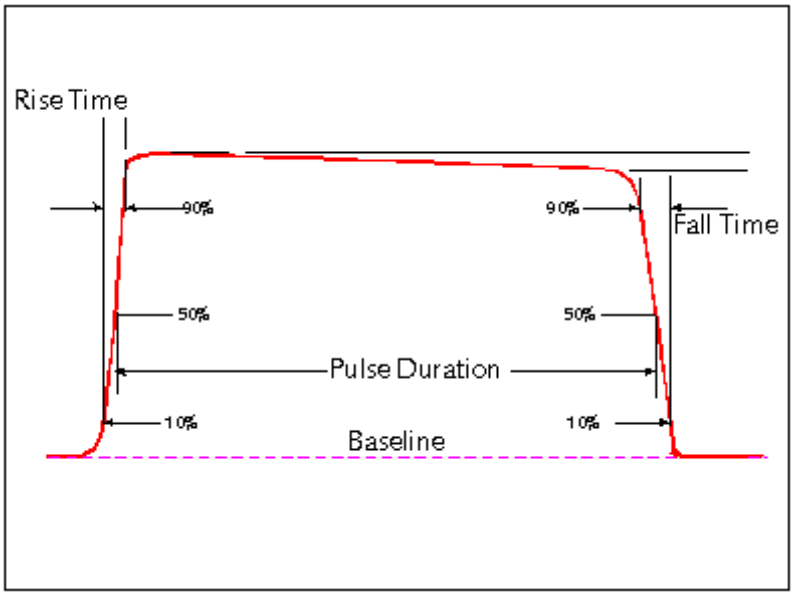


Figure 34: Clean Waveform

2.7.3.6.2. **Figure 34** shows an example of a clean pulse waveform at its source. This waveform is shaped with good rise and fall, without overshoot or undershoot.

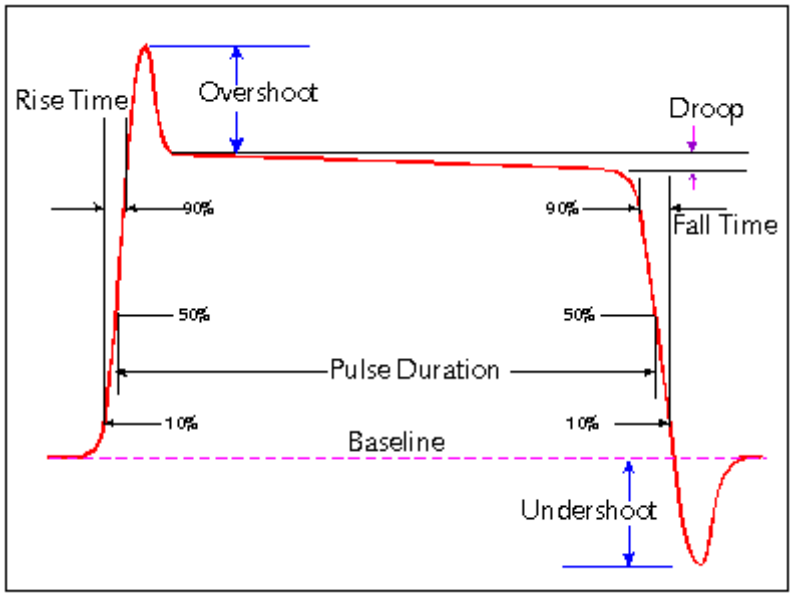


Figure 35: Waveform with Distortion

2.7.3.6.3. **Figure 35** shows an example of a waveform that exhibits overshoot and undershoot. These reflection conditions exist because of improper impedance matching. If this impedance mismatch is left in this state, it can cause erroneous effects to circuit performance, such as:

- Gate Latch-Up – When input voltages exceed the specified voltage for a logic family
- Output Current – Adds to inductive crosstalk and draws excess current
- Waveform Distortion – Affects propagation delays, varying rise time, and mismatched triggers

2.7.3.6.4. It is critical that all impedance requirements are defined *before* routing takes place. Impedance is controlled though modeling a board stack-up (see Layer Stack-Up section) and selecting a trace width, relative to the stack-up, that yields the proper impedance. By properly modeling the requirements of the signal, we can condition its environment for the best possible signal integrity.

2.7.3.7. Vias

2.7.3.7.1. Proper via selection is necessary to ensure that all design goals are achieved, and that the board can be manufactured. The selection of vias depends on board thickness, design technology, and the types of components used.

2.7.3.7.2. Vias are used for a variety of purposes. Some are for stitching power to internal planes, some for component fanout, and some for simple trace layer changes during routing. Therefore, a range of via sizes, rather than a single

size, is required for virtually all designs because of the different functions the vias perform.

2.7.3.7.3. Design requirements are constantly changing, and via technology is no exception. The discussion that follows provides as complete a guide as possible at the moment. Continued liaison with fabrication houses, particularly for leading-edge-technology designs, is an ongoing requirement.

*2.7.3.7.4. **Power Stitching***

2.7.3.7.4.1. This is commonly used in high-current designs, and where input and output voltages need to be connected to internal planes. The components used in these circuits are generally quite large, and this means there are usually some large areas around them where a surface layer plane can be used and a number of vias placed in that plane to stitch to an internal plane.

2.7.3.7.4.2. Although it is not the same 'stitching' use, these larger vias can often be used to connect large SMT tantalum capacitors to both power and ground planes on internal layers. The reasoning here is that the larger via will provide a connection to the plane that is less inductive and also capable of supporting higher current. Multiple vias are used to share the current load.

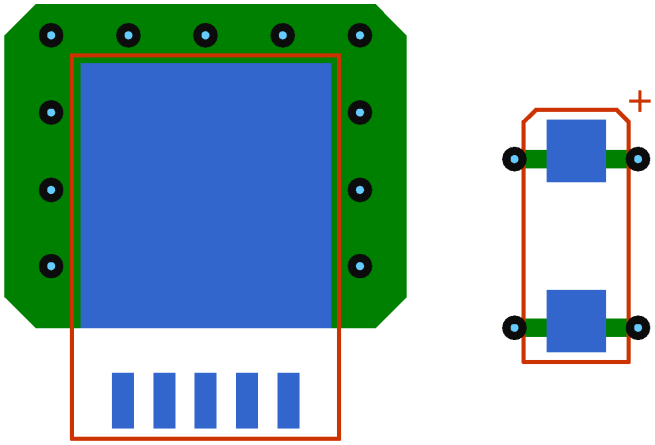


Figure 36: Power Stitching and Large SMT Cap. Connections

2.7.3.7.4.3. In the diagram (**Figure 36**), the regulator has its output pin buried in a surface layer plane and connected to the inner plane by the eleven large vias around it. In these circumstances a large via should be used for reduced inductance and resistance in the connection, and also for increased current capacity. This example uses a 45mil pad with a 20mil hole.

2.7.3.7.4.4. In the other example the capacitor is fanned out to the planes with two fanouts per pad, and each is connected with a separate trace. The vias are 35mil pads with 15mil holes. These traces should be 20mil wide or greater.

2.7.3.7.5. ***Thermal Pads***

2.7.3.7.5.1. Some SMD IC packages come with an exposed die pad on the bottom surface for enhanced thermal and electrical integrity. These die pads (sometimes called “slugs,” “exposed paddles,” or “thermal tabs”) allow the internal die to transfer heat effectively, as well as improve the electrical grounding. An exposed copper polygon, or Thermal Landing, must be provided on the surface of the PCB to facilitate this special pad. Thermal vias, typically placed as an array inside the polygon, conduct heat away from the IC.

2.7.3.7.5.2. IC application data may specify the thermal land pattern, as well as the minimum density, spacing, and drill diameter of the thermal vias. When reference data is unavailable the following rules-of-thumb should apply:

2.7.3.7.5.2.1. The thermal landing area should be at least as large as the IC die pad.
2.7.3.7.5.2.2. Exposed solderable copper area should clear the inside of the peripheral lands by at least 0.2mm.
2.7.3.7.5.2.3. Via diameter after plating should not exceed 10 mils, so as to prevent solder wicking during assembly. Anything larger should be tented or plugged.
2.7.3.7.5.2.4. Do not use web construction vias. Copper planes should always flood over thermal vias.
2.7.3.7.5.2.5. The die pad usually connects to one of the IC’s ground nets, so thermal vias should connect to internal ground planes.
2.7.3.7.5.2.6. Add copper to opposite side, if room permits.
2.7.3.7.5.2.7. Space vias in an array, typically on a 1mm-1.2mm grid.

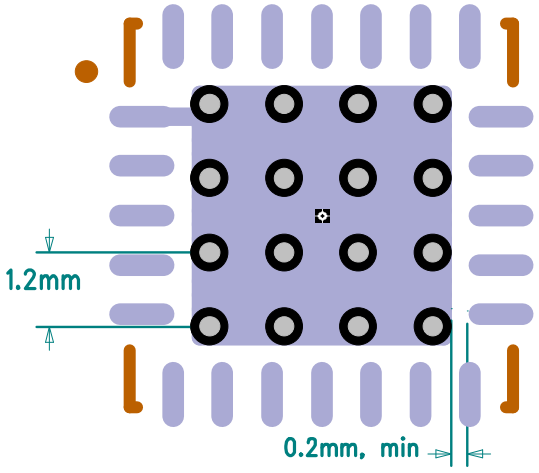


Figure 37: Thermal Pads

2.7.3.7.6. ***Fanout Vias***

2.7.3.7.6.1. Most components can be fanned out using the same via that is defined as the default via for routing the design. This should be determined on the basis of board thickness, taking into account the

aspect ratio[4] plating capabilities of the fabrication shop, and on the annular ring requirements given in the IPC Class 2 and Class 3 specifications (Reference IPC2221, ¶9.1.2). In most designs, these are easily defined and are 'standard' numbers used industry wide.

2.7.3.7.6.2. There are times, however, when a high density design requires many layers, forcing a thicker board, and this is when special care needs to be taken to check with the fab. house to find the allowable aspect ratio to use when the standard numbers simply do not apply. The following table lists 'standard' vias to use for different thickness boards. These are minimum hole size specifications and, as long as annular ring requirements are catered for, larger vias can usually be substituted based on the route channel needs of a particular design. Generally, the larger the via, the better, at least from a fabrication point of view.

Table 3: Via Hole Sizes to use for Multilayer Board without Microvia

	Board Thickness									
	0.031"		**0.063"**		**0.090"**		**0.110"**		**0.125"**	
Technology	Std.	High	Std.	High	Std.	High	Std.	High	Std.	High
Aspect Ratio	2.5:1	5:1	4.5:1	8:1	6:1	9:1	7.5:1	11:1	8.5:1	11.5:1
Via - Normal	13.5	8	13.5	8	13.5	10	14.5	10	14.5	11
Via – BGA1.27mm	13.5	8	13.5	8	13.5	10	14.5	10	14.5	11
Via – BGA1.0mm	12	8	12	8	12	10	12	10	12	11
Via – BGA0.8mm	10	6	10	8	µvia	10	µvia	10	µvia	11

(Based on TTM Technologies preferred rules as of January 2004)

2.7.3.7.7. ***Microvia***

2.7.3.7.7.1. The term, "microvia," is used to describe vias that are smaller than through vias, and which are normally drilled by laser. They span two or three layers, including one outer layer and, thus, are always blind, but never buried.

2.7.3.7.7.2. When microvia design is required, the microvias to use are based on the layer span and the thickness of material used for each layer. Microvias that span layers 1 to 2[5] can be smaller than those spanning layers 1 to 3. Also, since these layers are drilled and plated separately, there are fewer layers to align at this stage, so it is generally allowable to have a smaller hole-to-plane and annular ring clearance than for normal through vias. The following table lists some preferred microvia configurations.

Table 4: Via types for Microvia Designs

Layer Span

[4] Aspect Ratio = Board Thickness / *Finished* Hole Size

[5] Noted as "1:2" (or "*n*:*n*-1" for bottom-side microvias, where "*n*" is the number of layers).

	1:2[1]		1:3[1]	
Technology	Std.	High	Std.	High
Material Thickness (mils)	2.5	4	5	≥5
Laser Drill (mils)	6	4	8	7
Surface/Target Pads (mils)	14	10	16	12

Based on TTM Technologies preferred rules as of January 2004 [1]Note: 1:2 is the same as n:n-1, 1:3 is the same as n:n-2.

2.7.3.7.8. ***Soldermask***

2.7.3.7.8.1. The soldermask definition for vias should be approved by the customer, but often they will leave this parameter undefined and expect the designer to make the appropriate choices. The preferred approach is to *tent* all vias (that is, to cover the via with soldermask) on the primary side of the board, and to relieve the soldermask from the drills of all vias on the secondary side using the equation,

Bottom-Side Soldermask Relief = Drill size + .006 inch

2.7.3.7.8.2. This strategy protects the vias on the primary side of the design from creating shorts with exposed metal on parts being installed, and also reduces solder bridging that can occur during the assembly process. The secondary side soldermask relief also provides this protection, but allows access to the via for probing and rework. This also prevents the possibility of contaminants being trapped in the barrel of the via, which can then deteriorate the via barrel or “out-gas” during the assembly process.

2.7.3.7.8.3. Fanouts on BGAs should always have tented vias and drill relief regardless of other via parameters. In addition, bottom-mounted BGAs should have their vias tented on the bottom side (mount side), with the drill relief on the non-mount side for easy access to unreachable pins.

2.7.3.7.8.4. The customer, or the demands of the design itself, may require vias to be relieved of soldermask on both sides. If so, then the default minimum should be .002 inch beyond the pad size (i.e., pad size + .004 inch). Pay careful attention to your CAD tool’s settings for trace-to-via separation, to eliminate any possibility of trace exposure due to soldermask registration issues.

2.7.3.7.9. ***Route channels***

2.7.3.7.9.1. The vias used in a design will have a significant impact on available route channels on both external and internal layers. It is often necessary to allow more routing space between vias on internal layers than on external layers, particularly in BGA devices.

2.7.3.7.9.2. Today’s high speed designs are done with little or no routing on external layers, with the exception of fanout traces, and these should be kept as short as possible. Power supplies and other ‘static’ signals such as routing to DIP switches, LEDs and pullup/pulldown resistors on otherwise unused logic pins can usually be routed on external layers, and it is often an advantage to make sure these are routed on the surface layers as part of the fanout stage. This will result in fewer unnecessary vias being used in fanout, as long as there is at least one

for ICT, thereby increasing the number of available internal route channels.

2.7.3.7.9.3. Once we know the finished thickness of a board we can select the default and fanout vias for the design, based on the route density we have determined. If there are high pin count BGA devices, then the fanout vias for these devices needs to be analyzed to provide up to four traces between the vias on internal layers. It may be necessary to have some via padstacks in the library that have smaller internal layer pads than those on the external layers. This will make it easier for the fab. shop to fabricate, and also may provide that extra route channel you need.

2.7.3.7.9.4. The following table lists via sizes for BGA fanouts based on required route channels. These are specified as maximum INTERNAL layer pad sizes for the vias and the correct via padstacks need to be selected based on board thickness, annular ring (Note 2), and aspect ratio capabilities of the fab. shop. External layer pad sizes are determined in conjunction with the design via-to-pad spacing and minimum annular ring rules.

2.7.3.7.9.5. Routing rules are defined as space1 (S1) / trace (T) / space2 (S2), where space1 is trace to via and space2 is trace to trace. Microvia is denoted in the table as *µx* in the Via Pad column(s), where *x* is the diameter of the microvia pad.

2.7.3.7.9.6. Use the drawing in **Figure 38** in conjunction with the table below, where:

T = Trace Width

S1 = Trace-to-Via spacing (Note 3)

S2 = Trace-to-Trace spacing (Note 4)

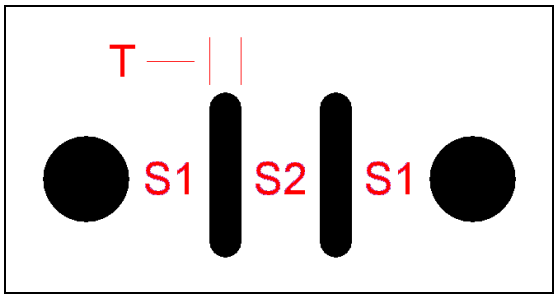


Figure 38: Route Channel Graphic

Table 5: BGA Route Channel Chart

BGA / Rules	1 Trace	2 Traces	3 Traces	4 Traces
1.27MM – 6/6/6	32	20	N/A	N/A
1.27MM – 5/6/6	34	22	μ10	N/A
1.27MM – 5/6/5	34	23	μ12	N/A
1.27MM – 6/5/6	33	22	μ11	N/A
1.27MM – 5/5/6	35	24	μ13	N/A
1.27MM – 5/5/5	35	25	μ15	N/A
1.27MM - 5/4/5	36	27	18	N/A
1.27MM – 4/4/5	38	29	20	μ11
1.27MM – 4/4/4	38	30	22	μ14
1.27MM - 4/3/4	39	32	25	18
1.27MM – 3/3/4	41	34	27	20
1.27MM – 3/3/3	41	35	29	23
1MM – 6/6/6	21.3	N/A	N/A	N/A
1MM – 5/6/6	23.3	11.3	N/A	N/A
1MM – 5/6/5	23.3	12.3	N/A	N/A
1MM – 6/5/6	22.3	11.3	N/A	N/A
1MM – 5/5/6	24.3	13.3	N/A	N/A
1MM – 5/5/5	24.3	14.3	N/A	N/A
1MM – 5/4/5	25.3	(μ)16.3 (Note 5)	N/A	N/A
1MM – 4/4/5	27.3	18.3	N/A	N/A
1MM – 4/4/4	27.3	19.3	μ11.3	N/A
1MM – 4/3/4	28.3	21.3	μ14.3	N/A
1MM – 3/3/4	30.3	23.3	(μ)16.3	N/A
1MM – 3/3/3	30.3	24.3	18.3	μ12.3
0.8MM – 6/6/6	μ13.5	N/A	N/A	N/A
0.8MM – 5/6/6	μ15.5	N/A	N/A	N/A
0.8MM – 5/6/5	μ15.5	N/A	N/A	N/A
0.8MM – 6/5/6	μ14.5	N/A	N/A	N/A
0.8MM – 5/5/6	(μ)16.5	N/A	N/A	N/A
0.8MM – 5/5/5	(μ)16.5	N/A	N/A	N/A
0.8MM – 5/4/5	(μ)17.5	N/A	N/A	N/A
0.8MM – 4/4/5	19.5	μ10.5	N/A	N/A
0.8MM – 4/4/4	19.5	μ11.5	N/A	N/A
0.8MM – 4/3/4	20.5	μ13.5	N/A	N/A
0.8MM – 3/3/4	22.5	μ15.5	N/A	N/A
0.8MM – 3/3/3	22.5	(μ)16.5	μ10.5	N/A

Notes:

1. All the values in the above table are calculated using TTM Technologies preferred rules as at January 2004 and specified in the preceding tables.
2. Annular ring – IPC Class 2 = drill + 10mils; IPC Class 3 = drill + 12mils.
3. Trace-to-via spacing should be reduced before trace-to-trace spacing because trace-to-via is a point clearance, whereas trace-to-trace is continuous.
4. Trace-to-trace spacing should be maintained at a value equal to or (preferably) greater than the vertical distance from the traces to the nearest plane. This significantly improves crosstalk characteristics.
5. Vias with 16mil pads can be used with a 6mil mechanical drill if the finished thickness of the board is 0.031 inches or less, otherwise any vias with pads less than 18mils are microvias. These are shown in the table with the microvia 'μ' in parenthesis.

2.7.3.7.10. ***Power Planes***

2.7.3.7.10.1. Before we can say that we have defined the padstack for a given via on a particular design, we still need to consider the impact of these vias on internal power and ground planes. Because the fabrication requirements dictate the minimum hole-to-plane spacing, we need to consider this as well. If the combination of this spacing requirement and the via pitch used in the design causes these internal planes clearance pads to overlap, then we will have a situation where a 'slot' will be created in the planes. If, at the same time, the via pitch and the routing spacing rules are such that there can be traces routed on internal layers between these vias, then there will be an interruption to the return path for these signals. Overlapping via clearance pads will create the slot in the plane and force the return currents to 'go around' this slot. This is one of the most significant causes of signal integrity problems in multilayer PCBs, and must be avoided.

2.7.3.7.10.2. The problem can be resolved by either reducing the internal plane layer pads on the vias, or by increasing the spacing between the vias. When the vias in question are in a BGA grid, we cannot do anything about the via spacing, so we need to be able to use a smaller hole size. This will then result in a smaller clearance pad being required. Of course, a smaller hole can only be used if it is within the available aspect ratio capability.

2.7.3.7.10.3. Changing the material specification used in the stack-up can result in a thinner board, allowing a smaller hole to still fit within the aspect ratio specifications, as long as a thinner finished board is allowable.

2.7.3.7.10.4. Reducing the trace widths and spacing rules can give an increase in the route channels available which, in turn, can reduce the number of layers required and result in a thinner board, smaller hole and smaller clearance pad. If full consideration is given to all these alternatives and a suitable via padstack still cannot be determined, then you may need to investigate the possibility of using microvia technology.

2.7.3.7.10.5. You can see that there are numerous ways to resolve this problem, but it must be resolved.

2.7.3.7.11. ***Via Cap and Plug***

2.7.3.7.11.1. Via capping and plugging are secondary processes that protect vias and improve their characteristics in a variety of different application needs. Designers must make some adjustments in the layout to accommodate these processes and to prevent any production delays. Some additional output data and fabrication notes may be required, depending on the process and material used.

2.7.3.7.11.2. Via Cap

2.7.3.7.11.2.1. Via capping is a secondary application of soldermask over just the via drill holes in order to seal or "cap" them on one side of the board. This typically covers the entire via leaving no exposed copper, and creating good isolation between all components, solder, or other exposed metal. In the special case of thermal pads (i.e., heat slugs), it also prevents solder from flowing through any via holes located within the thermal pad area. The via capping process is typically applied to the primary side of

the board, or whichever side contains the highest number of active components. It is applied after the PCB has been constructed, plated, covered with soldermask, and after receiving its final coating finish, such as Gold Immersion or HASL.

2.7.3.7.11.2.2. The via to be capped must have a soldermask opening defined with a minimum size of .006" over the drill size on both sides of the PC board, however, only one side of the via is capped. After the via cap has been applied, the other side of the via hole must remain open. This prevents air or contaminates from being trapped inside the hole, which can lead to “out-gassing” or corrosion of the via barrel.

2.7.3.7.11.2.3. The via cap data may be communicated to the fabrication house either by sending a Gerber layer showing all via holes along with the rest of the output data, or by adding a fabrication note to the fab drawing, specifying the process to be used and which side of the board to cap.

2.7.3.7.11.3. Via Plug

2.7.3.7.11.3.1. Via plugging is the process of inserting additional material into the drill hole of a via. The inserted material may be either conductive or non-conductive depending on the needs of the application. Some common uses of via plugging are to increase thermal and electrical conductivity, to ensure that vias are flush to the surface when located within an SMD pad, and to prevent contaminates and moisture from entering the via hole. Via plugging can be done at different stages toward the end of the fabrication process, but will typically be applied after the board has been constructed and processed for its final coating finish (Gold Immersion, HASL).

2.7.3.7.11.3.2. Similar to the via capping process, the soldermask opening should be a minimum of .006" over the drill size on both sides of the PC board.

2.7.3.7.11.3.3. The via plug data may be communicated to the fabrication house either by sending a Gerber layer showing all via holes along with the rest of the output data, or by adding a fabrication note to the fab drawing, specifying the process to be used.

2.7.3.7.11.4. The fabrication house may modify these via cap and via plug Gerber files in order to accommodate their internal processes, but this will provide them with guidance on where to focus their efforts accurately.

2.7.3.7.12. ***Summary***

2.7.3.7.12.1. Once we have calculated all the above information and factored in any appropriate manufacturing and/or customer standards, we will arrive at the parameters that we can use for a via padstack that will best satisfy the requirements for a given design. All the factors that affect the final via padstack selection must be taken into account when determining what vias to use.

2.7.3.8. Net Ordering

2.7.3.8.1. Net ordering is used to define the sequence and pattern in which a signal is connected to each device in a design. Different patterns are used to allow the designer to control the designs' intent, and a way to provide rules for the signal path to follow. Net ordering can be used to help define a memory bus so that each signal routes to each device in the same sequence, to force the termination pin to be the last load on a clock signal, or to eliminate any stubs on a high speed signal path. There are several common methods for Net Ordering a signal path: Minimum Spanning Tree (MST), Chained, Forced, Star, and T-Junction. (See Figure 39 through Figure 43.)

2.7.3.8.1.1. Minimum Spanning Tree (MST), also known as "free," is the default for any nets not specified. This means nets can be connected in any fashion.

2.7.3.8.1.2. Chained, also known as "Daisy-Chained," the signal connects in the quickest and most direct sequential series fashion with no branches or stubs.

2.7.3.8.1.3. Forced, the signal connects in custom sequence defined by the designer and will typically be a series fashion with no branches or stubs.

2.7.3.8.1.4. Star, the signal routes to a central point at which several branches extend to each load, each branch typically equal in length.

2.7.3.8.1.5. T-Junction, similar to a Star net ordering, the signal routes to a central point at which two branches extend to each load, each branch typically equal in length.

2.7.3.8.2. Minimum Spanning Tree (MST)

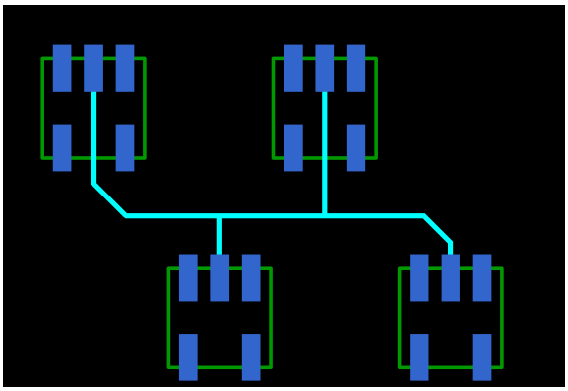


Figure 39: Minimum Spanning Tree (MST)

2.7.3.8.3. Chained

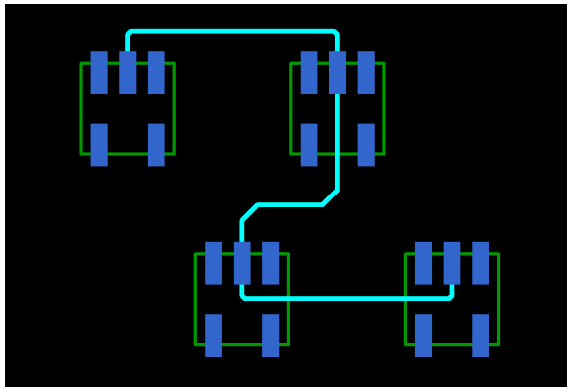


Figure 40: Chained

2.7.3.8.4. Forced

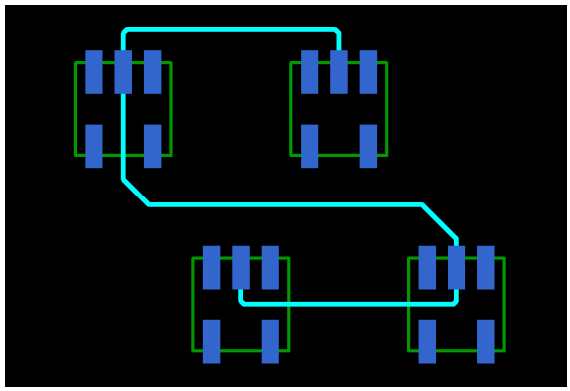


Figure 41: Forced

2.7.3.8.5. Star

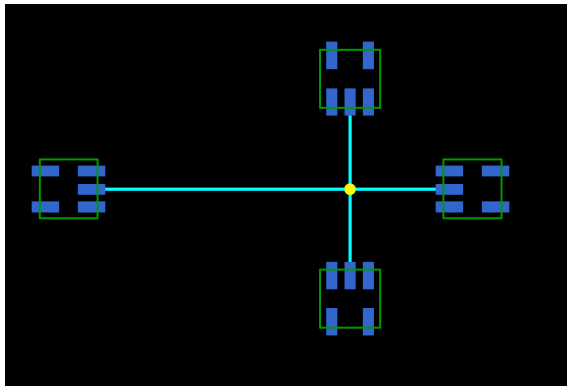


Figure 42: Star

2.7.3.8.6. T-Junction

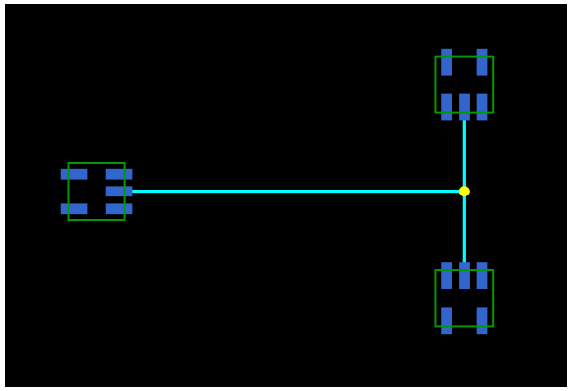


Figure 43: T-Junction

2.7.3.9. Pairs

2.7.3.9.1. Differential pairs, two traces routed adjacent to each other as a "pair," are common to most designs and must follow some general guidelines to achieve their intent. They are often driven with strict impedance and length requirements so they should be considered early in the layout of your design.

2.7.3.9.2. The two types of differential pair routing are inductive and broadside (as shown below in these profile views):

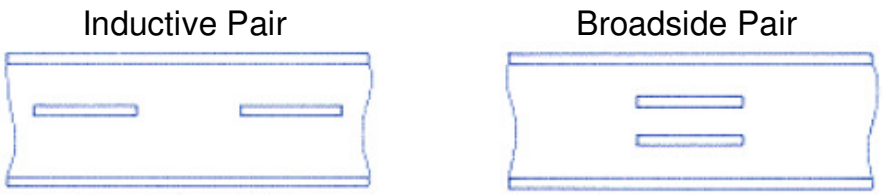


Figure 44: Inductive and Broadside Differential Pairs

2.7.3.9.3. In a differential pair, each conductor carries a voltage and current that is equal and opposite the other. The magnetic fields produced by the equal and opposite currents cancel each other which help to reduce EMI, and to reject any external noise introduced during its travel through a cable or PC Board. The unwanted noise that is introduced from other sources will couple equally into each conductor resulting in a common mode rejection of that noise. These characteristics are highly desirable and will continue to drive the need for differential pairs.

2.7.3.9.4. The key elements to designing a good differential pair are equal lengths within the pair (known as "intra-pair skew"), keeping the pair adjacent to each other, consistent impedance, and proper termination (when needed). It is important to understand how to control these parameters so that the best performance can be obtained from the differential pair. A critical consideration to keep in mind is where to add length to one conductor of a differential pair in order to make their intra-pair lengths match. It's critical that the length is added at the end (destination) of the differential pair, and not at the beginning (source). This allows the signal to travel the length of the trace and reach its destination in phase with its respective pair. See **Figure 45** for examples. The additional length should only be added at the end where the pair is forced to separate.

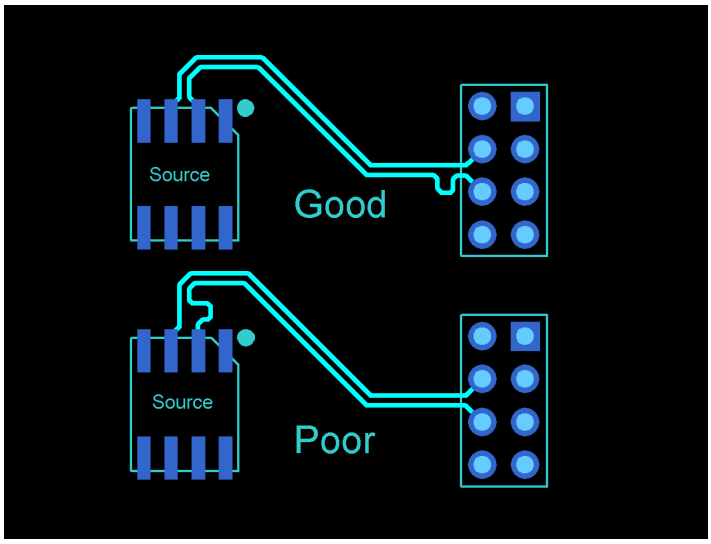


Figure 45: Intra-Pair Length Matching

2.7.3.9.5. The following general spacing requirements should be used unless otherwise specified.

Edge Coupled Pairs	Broadside Coupled Pairs
Microstrip: 4Mil x Dielectric	Microstrip: 3Mil x Dielectric
Stripline: 3Mil x Dielectric	Stripline: 2Mil x Dielectric

*2.7.3.9.6. **Inductive***

2.7.3.9.6.1. Inductive pairing, also known as “edge-coupled” or “same-layer” pairs, is the most common method used. Many times this is used because there is no need for a broadside structure. Therefore, by default, this is the choice routing method.

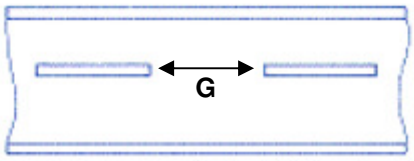


Figure 46: Inductive Pair Gap

2.7.3.9.6.2. Referring to the above drawing, inductive pairing uses the gap (G) between two copper traces to isolate the two signals. Inductive is preferred, when there are only a few pairs to be routed, or when density is low. The benefit is that it does not take two adjacent layers to route, therefore is not as demanding on stack-up requirements.

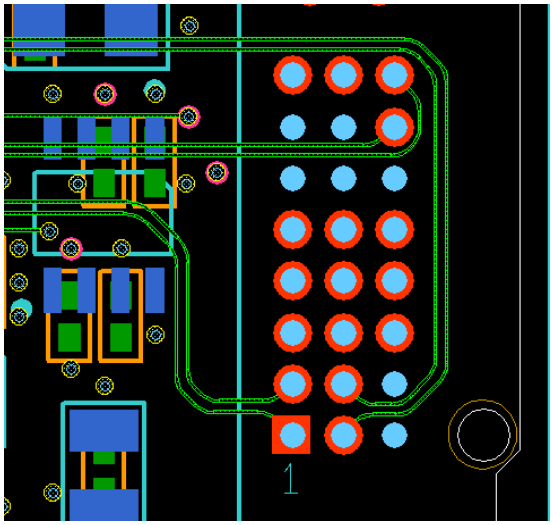


Figure 47: Example of Routed Inductive Pairs

2.7.3.9.6.3. Signal pairs traveling into the connector (as shown in the above diagram) have been routed using inductive pairing.

*2.7.3.9.7. **Broadside***

2.7.3.9.7.1. Broadside pairing is also known as “adjacent-coupled” or “opposing-layer” pairs. Although not widely used, broadside pairing does serve a very specific purpose—routing where many pairs exist and space is limited. For example, one might want to use broadside pairing when a design requires extremely high density, with a high number of route pairs, e.g., network backplanes. Broadside is very useful in this situation, because in most instances, many pairs are trying to enter or exit the PCB. These signals must travel through high-density, controlled-impedance connectors, where it is impossible to route the number of controlled pairs without this type of routing.

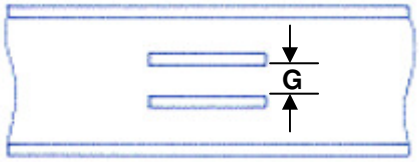


Figure 48: Broadside Pair Gap

2.7.3.9.7.2. Referring to the above drawing, broadside uses the dielectric material between two copper layers to isolate the pair (G). This makes it more difficult to model the stack-up, since the dielectric of the board material affects the coupling of the signals. Also, it is much more difficult for the fabricator to achieve the target impedance specification due to the processes involved in laminating the PCB.

2.7.3.9.7.3. The good news for the designer is that since the signals are “stacked”, the pair takes less routing space, which increases density. Also, productivity increases, since the traces are directly atop each other (except where they must split at terminations). Once the first trace is routed, the second is practically a copy of the first, and with

most routing tools, the second trace is routed simultaneously as the first is drawn.

2.7.3.9.7.4. The advantages of broadside include the increased coupling of signals, and minimum skew in trace lengths.

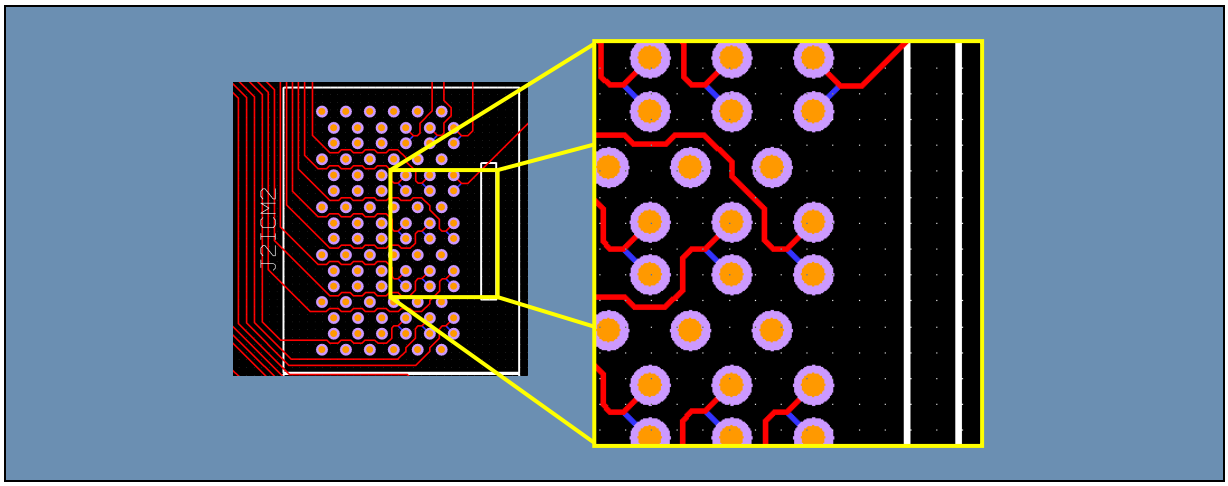


Figure 49: Broadside Signal Pairs Diverging at Endpoint

2.7.3.9.7.5. Signal pairs traveling into the connector (as shown in the above diagrams) have been routed using the broadside method, and demonstrate tight coupling while remaining equal in length.

2.7.3.9.7.6. Before routing any PCB traces, generally it is a very good idea to plan ahead when designs require pairing. Below is list of things that should be considered:

2.7.3.9.7.6.1. The nets which make up pairs must be defined as pairs. Tools aid in proper assignment and control of pair nets.

2.7.3.9.7.6.2. Does the design have the number of pairs and density that will require broadside pair routes? If so, this must be accounted for in the stack-up.

2.7.3.9.7.6.3. What layers are available for pairs to route? This must be accounted for in the stack-up. This should also be defined in tools to aid in proper control of pair nets.

2.7.3.9.7.6.4. What impedance requirements are applied to the pairs? What trace width and space (dielectric) are required to achieve the desired impedance?

2.7.3.9.7.6.5. Will we need to maintain separation between pairs and other nets? This should also be defined in tools to aid in proper control of pair nets.

2.7.3.9.7.6.6. Make sure there is a reference plane or plenty of air-gap between pairs on adjacent layers. If this rule is ignored, massive crosstalk can be seen.

2.7.3.9.7.7. With all these concerns and issues to be dealt with, it is a very good idea to address them at the earliest possible point in the design (even before placing parts). By doing so, costly re-design can be avoided. It is also almost mandatory to deal with signal pairs first in the route cycle, followed by securing them, so no further edits can modify them.

2.7.3.10. Timing

2.7.3.10.1. Timing is becoming more and more critical to proper routing. Generally, timing is a consideration due to data length/delay vs. clock length/delay. Common methods of controlling signal timing include:

2.7.3.10.1.1. **Max. Length** Maximum length is a constraint applied to signals which will either lose amplitude, are suspect to crosstalk, or are feared to have excess capacitance. Maximum length generally can be applied to many nets or groups. Layout tools usually offer methods for entering and controlling this requirement.

2.7.3.10.1.2. **Match Length** Matched length is generally used when a design has a bus that must be synchronized to a clock signal. Lengths usually are specified to route equal in length to the longest signal of a group. Additional length is added to the shorter traces, by allowing the net to wind in a serpentine fashion. Layout tools usually offer methods for entering and controlling this requirement.

2.7.3.10.1.3. **Delays** Delays control the amount of time that a signal takes to get from one pin to another. An example of this is the PCICLK signal on a PCI Board. The PCI Specification calls for the PCICLK signal to be 2.5 inches (or .42 nanoseconds) long. So unless the part is placed so that the routed trace is exactly 2.5" (and it is not allowed to be longer), then this signal must be delayed by at least a small amount.

2.7.3.10.2. **Figure 50** shows the additional length added to this signal using the serpentine routing method.

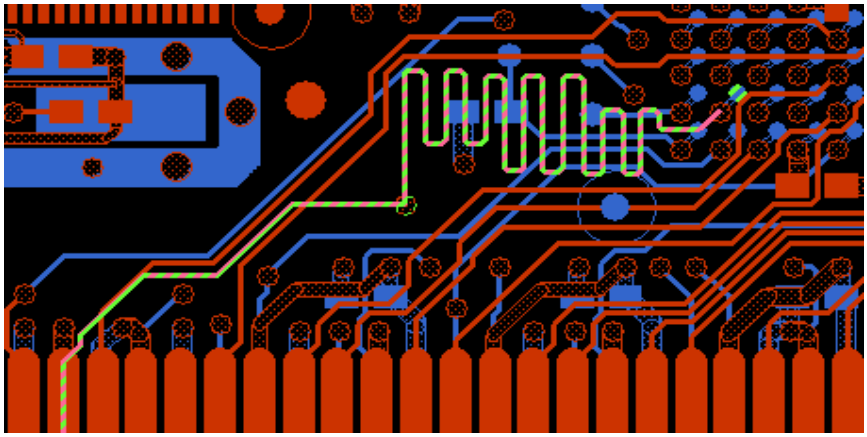


Figure 50: Serpentine Routing

2.7.3.10.3. Other examples of delays include when one signal must match another signal *plus* a specified amount of either length or delay. For example, if Clock_B must equal Clock_A plus 1ns, and if Clock_A is 2.50" (.42nS), then

the length of Clock_B must be 1nS of length (5.95") added to Clock_A's length, for a total of 8.45".

2.7.3.10.3.1. Clock_B = Clock_A + 1nS

2.7.3.10.3.2. Clock_B = .42nS + 1nS

2.7.3.10.3.3. Clock_B = 2.50" + 5.95"

2.7.3.10.3.4. Clock_B = 8.45"

2.7.3.10.4. Delay requirements sometimes include signals that have a component in series:

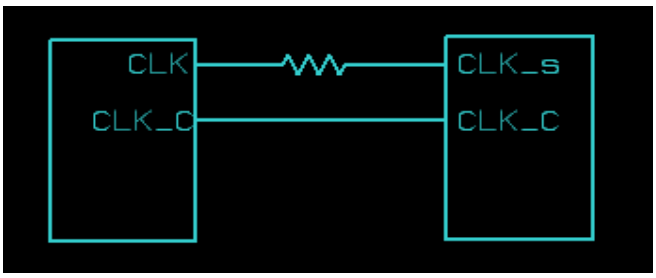


Figure 51: Schematic Example of Delay with Series Resistor

2.7.3.10.4.1. Example: Clock_C = Clock + Clock_s

2.7.3.10.4.2. The layout may look something like this:

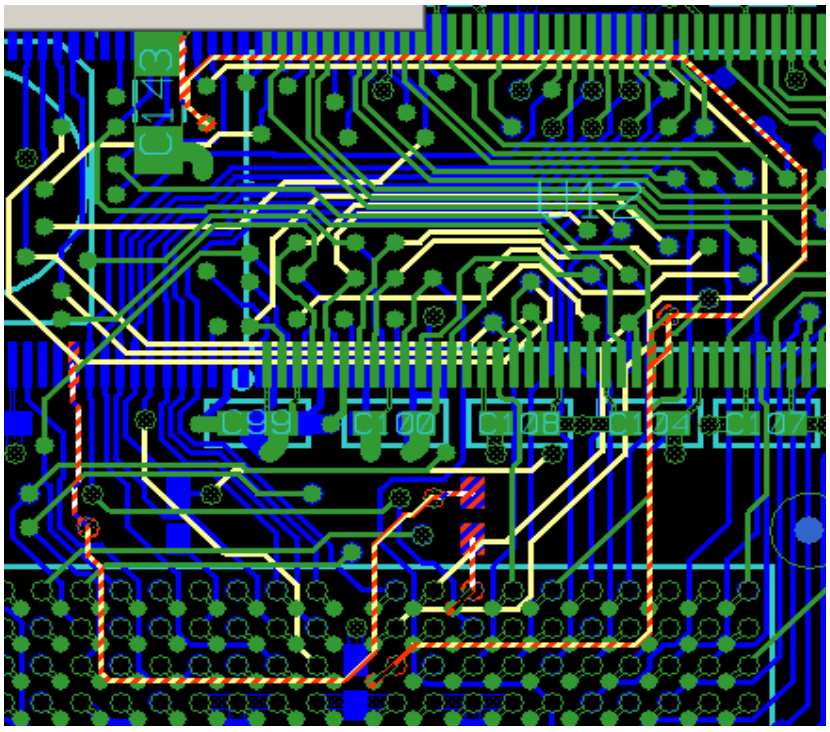


Figure 52: Example of Route using Delay Requirement with Series Resistor

2.7.3.10.4.3. In this case the signal lengths are:

[Clock = 1.30" + Clock_s = .10"] = Clock_C at 1.40"

2.7.4. Maximum Via Count per Net

2.7.4.1. Maximum via count, in some instances, is very important. As the name implies, it limits the number of vias allowed on a net. For example, there may be a need to route signals making only one layer-to-layer transition (two vias maximum), or for a signal to route fully on one layer (zero vias).

2.7.4.2. Maximum via count helps to meet these rules and to control the effects that vias can have on signal integrity. These effects include capacitive loading, a change in impedance, and possible reflection in high speed signals. Drill costs are also reduced. Often many critical layouts will require routing without vias to avoid these issues. Tools can aid and verify if there is a presence of more vias than specified, which must be addressed to meet the rule.

2.7.4.3. One tip to keep in mind -- Set the rule in your CAD tool (if possible) *before* routing, as trying to clear errors after traces have been placed may cause much painful re-design.

2.7.5. Pin and Gate Swapping

2.7.5.1. In order to have a clean route, occasionally the designer may have to swap pins or gates on some devices. Usually the devices that require pin or gate swaps include resistor networks, capacitor networks, gated ICs (such as buffers), inverters, analog gates, and occasionally FPGAs. In every case the designer must consult with the engineer and get permission to make any changes. After making any changes, the information must be fed back to the engineer in the form of a Was/Is list or marked-up schematic, so that the schematic may be updated.

2.7.5.2. Pin Swapping

2.7.5.2.1. Pin swapping is when the individual pins of a single device are swapped. Typically this is done on resistor networks. **Figure 53** is an example of swapping pins 4 and 5, and pins 3 and 6.

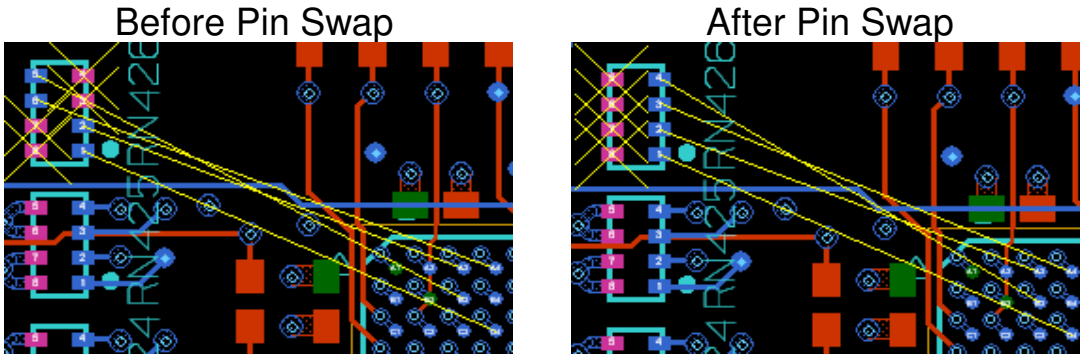


Figure 53: Pin Swapping - Before and After

2.7.5.3. Gate Swapping

2.7.5.3.1. Unlike pin swapping, which is the swapping of individual like pins (e.g., bi-directional or I/O pins) within the same package, gate swapping is the swapping of one or more pins (combination of input, output, etc. pins that make up a circuit) within the same package or another package that is of the same part number. When gate swapping, be sure to consult the datasheet of the part number to ensure that the gates of a device are indeed compatible, and to verify how the device is pinned out.

2.7.5.3.2. **Figure 54** shows a resistor network being gate swapped within the same package. The four gates in this case are pins 1 and 8, 2 and 7, 3 and 6, and 4 and 5.

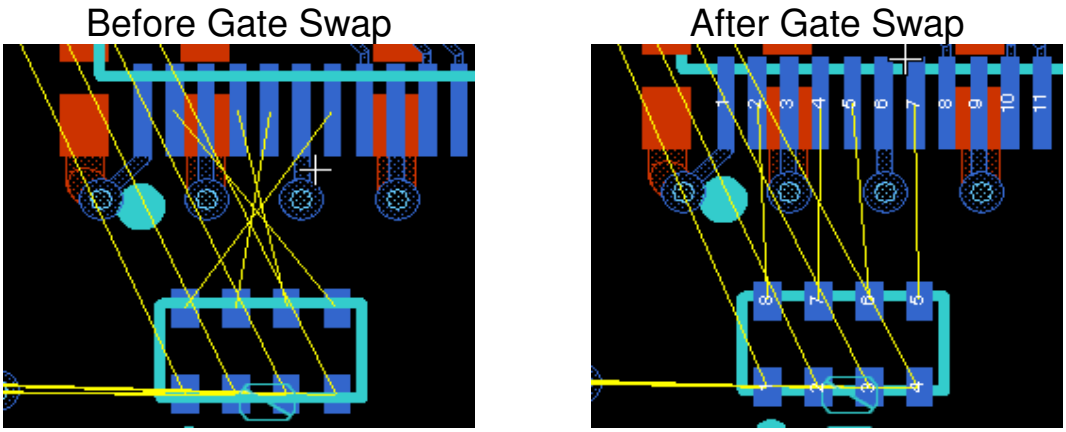


Figure 54: Gate Swapping (Within Package) - Before and After

2.7.5.3.3. **Figure 55** shows a resistor network being gate swapped between packages (RN414 and RN415)

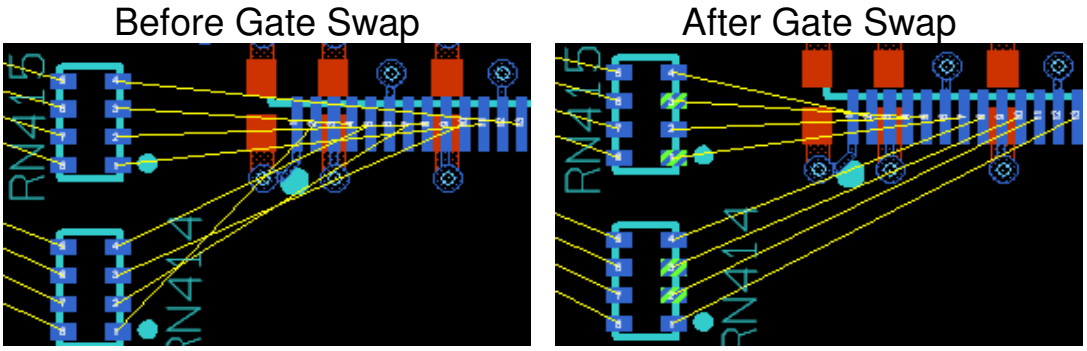


Figure 55: Gate Swapping (Between Packages) - Before and After

2.7.6. Fanout

2.7.6.1. "Fanout" is the process of connecting the signal and power pins of surface mount devices (SMDs) to vias, in order to make them available to internal signal layers for routing, and internal power and ground planes, respectively. The fanout *stage*, however, does not mean "add a fanout to each and every SMD pad." It means fanning out where appropriate, and connecting short traces with no via, if they do not need to have a testpoint attached.

2.7.6.2. After all the necessary fanouts have been placed (and only necessary fanouts), then they are locked down to prevent them from being moved, to reduce bad trace pad entries, and other possible problems that can be created in the routing stage.

2.7.6.3. Fanout is also an integral part of the overall ODA In-Circuit Test (ICT) testpoint generation strategy. (See *ICT / Flying Probe Testpoints* section on page 76.)

2.7.6.4. *Order of Fanning Out Devices*

2.7.6.4.1. Power and ground pins should be fanned out first, with traces kept as short and wide as possible, particularly the ground pin traces. Longer and thinner traces are more inductive and can give rise to ground noise or an increased ground potential, causing what is known as 'ground bounce' in digital circuits. This has the potential to completely disrupt circuit functionality and, in some severe cases, can even cause permanent component damage.

2.7.6.4.2. Clocks and high speed signals should be fanned out next, followed by non-critical signals.

2.7.6.4.3. On fine pitch components, such as QFP packages, it is preferable to align the fanout vias in rows or columns. This will give the minimum amount of meandering in traces routed in the gaps between vias as well as reducing the blockage of available route channels.

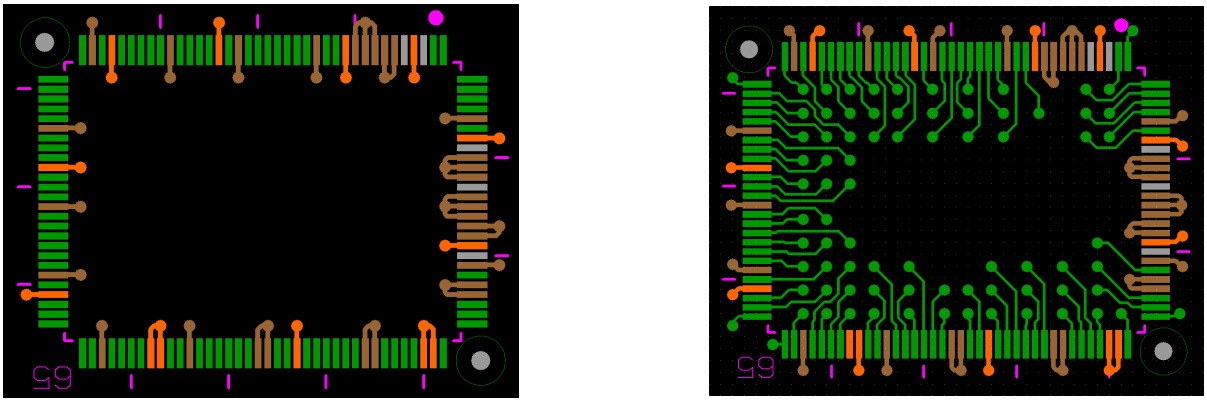


Figure 56: QFP Power Fanout, and Power and Signal Fanout

2.7.6.4.4. Notice in **Figure 56** that power and ground is fanned out first in order to keep these connections as short as possible. Then signal pins are fanned out in a row and column via grid to present the least disruption of inner-layer route channels.

2.7.6.4.5. The choice of via grid depends on the ICT technology in use, if any, and may be set to either 50 mils or 75 mils. In the case of flying probe ICT, 50 mils is adequate. For bed-of-nails ICT, 75 mils is preferable, but 50 mils is allowed.

2.7.6.4.6. If signals are bussed or otherwise connected to multiple devices with a 50 mil via grid (i.e., each signal has multiple opportunities for the placement of testpoints), then 70 mil ICT spacing can be easily achieved by using only alternate vias on each device as ICT sites.

2.7.6.5. *Eliminate Unnecessary or Excessive Fanouts*

2.7.6.5.1. Not all SMT pads need to have a fanout via. There are many cases of series termination resistors, pullup or pulldown resistors, short connections, etc., where only one via is required for ICT purposes or, if ICT is not required, no vias are needed at all. Fanning out unnecessary SMT pins will result in blocked internal layer route channels. This will make it much more difficult to route high density digital designs, and will also largely reduce your ability to tune traces in heavily constrained designs. Good placement and economical use of fanout vias will help significantly when routing these types of boards.

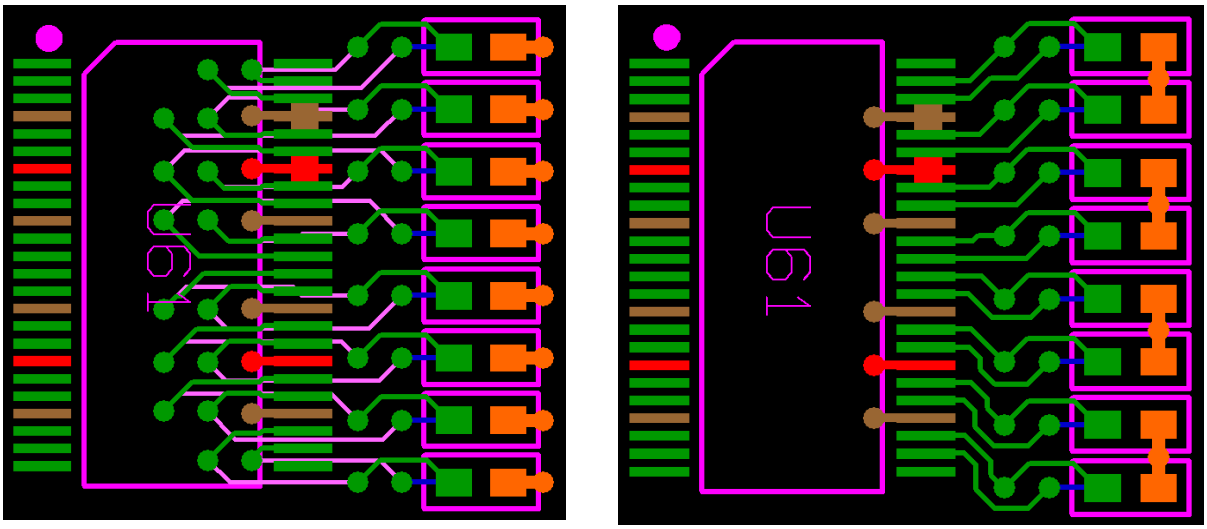


Figure 57: Eliminating Excessive Vias

2.7.6.5.2. Notice in the left hand illustration in **Figure 57** that there are forty vias used for only sixteen data bits and pullup resistors. This is what will happen if all pins are individually fanned out prior to routing. By noticing the net lines and being aware that these are short connections, you can easily reduce the number of vias to the result shown in the right hand figure. Now there are only twenty vias used to produce the same result, while maintaining full ICT capability. The power side of pull-up and pull-down resistors may commonly share vias.

2.7.6.5.3. The arrangement on the right is a much cleaner solution for a number of reasons. Firstly, having twenty fewer vias will result in much less blockage of internal layer route channels. There is no need to use an internal layer for routing U61 to the resistors, so this already makes more internal route space available.

2.7.6.5.4. Secondly, the traces connecting to the pull-up resistors are all considerably shorter.

2.7.6.5.5. Lastly, it provides for better signal integrity by eliminating the added capacitance that a via presents to a signal, eliminating a potential stub from the internal signal layer to the surface of the board.

2.7.6.6. High Current Fanout Techniques

2.7.6.6.1. When using multiple vias for fanout of high current traces, try using either a plane shape or a separate trace from the pad to each via. Using only one trace to multiple vias is more inductive and has less current capacity. Capacitor A shows a typical fanout using multiple vias but only one trace to the component pad. Avoid this. Capacitor B shows the same number of vias but with separate traces to the component pad. This is what should be done the majority of the time. Capacitor C shows the component pad buried in a surface layer plane shape (the plane shape is not shown) with multiple vias stitching to an internal plane layer. Use this method in power supply areas.

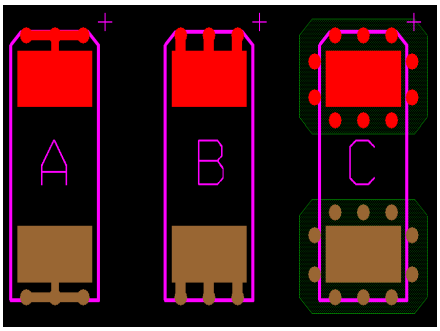


Figure 58: Multiple Vias For Power Pads

2.7.7. ICT / Flying Probe Testpoints

2.7.7.1. During the pre-layout interview, it is important for the designer to understand how the board will be tested after assembly. By knowing if the board will be In-Circuit Tested (ICT), Flying Probe, or not tested at all, the designer can make the informed decision on what rules will be applied to placing testpoints. As mentioned previously under the heading, “Fanout,” vias play an integral part of the overall ODA ICT testpoint generation strategy. ODA designers must ensure that they can achieve 100% testpoint coverage at the time of fanout completion before routing the rest of the board. By waiting for a board to be routed before adding testpoints, you can make an easy task difficult or nearly impossible. The following two sections discuss the fundamental differences between ICT and Flying Probe.

2.7.7.2. ICT

2.7.7.2.1. ICT has been in use for many years. This method of testing not only looks at short circuits, open circuits, and component values, but it also checks the operation of ICs.

2.7.7.2.2. In ICT, spring-loaded probes are inserted on a “bed-of-nails” plate through holes drilled in it at the same position as the testpoint locations (nodes) designated in the design database. When it is tested, the board is placed on top of the bed of nails test fixture, and pressed down by a press plate, making contact between the board and the probes. The board is then tested by the automated test equipment (ATE), as various signals are sent through the probes to the board’s circuitry.

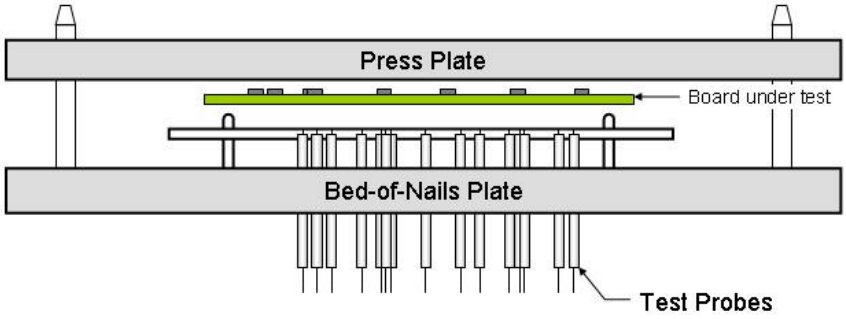


Figure 59: ICT Bed-Of-Nails

2.7.7.2.3. Although a very powerful tool in today’s high density board factors, it is limited by lack of nodal access by way of the bed-of-nails fixture. Pins of the

bed-of-nails fixture must be accurately placed to make good contact with the nodes on the board. In view of this, and the increasing number of nodes being found on many boards today, it is being used less than in previous years, although it is still widely used.

Table 6: Summary of ICT Advantages and Disadvantages

Pros	Extremely fast (once programmed) Highly stable Excellent for long term and high volume products Test results are easily interpreted
Cons	Programming and fixture builds are expensive and time consuming Very difficult to achieve 100% nodal access

2.7.7.2.4. Designers should adhere to the following rules for ICT:

2.7.7.2.4.1. **Testpoint Side—**Although boards can be tested from both sides of the board (clamshell), the high cost makes it prohibitive to do so. ODA standard is to place all testpoints on one side of the board (usually the bottom) so that testing costs may be minimized.

2.7.7.2.4.2. **Testpoint Size and Shape—**Standard testpoint size and shape is .032" Round.

2.7.7.2.4.3. **Test Target Type—**Although testpoints may be physically placed anywhere on the board, there are some places where testpoints are preferred. They are classified as “test target types,” and are listed below, in order of preference–

2.7.7.2.4.3.1. Through-Hole Component Leads

2.7.7.2.4.3.2. Vias

2.7.7.2.4.3.3. Gold Fingers

2.7.7.2.4.4. Testpoint-to-Testpoint Clearance

2.7.7.2.4.4.1. The standard TP-to-TP clearance is .075" from center-to-center, and all testpoints should be placed according to this rule.

2.7.7.2.4.4.2. However, there may be some flexibility regarding the standard spacing. If 100% coverage is critical to the design, but is not achieved at the standard spacing, and if most nodes have testpoints (say >85%), it may be permissible to place the remaining testpoints at a clearance of .050" center-to-center.

2.7.7.2.4.4.3. Reducing the standard TP-to-TP clearance may only be done on a case-by-case basis, where the added coverage is deemed by the customer to be worth the extra testing costs incurred as a result of the tighter tolerances involved.

2.7.7.2.4.5. Minimum Number of Testpoints, by Node Type

2.7.7.2.4.5.1. Signal Node = 1

2.7.7.2.4.5.2. Power Node = May require 2 or 3, depending on board size and the usage of the plane

2.7.7.2.4.5.3. Ground Node = Evenly distributed across the board, for example, on a 2-inch grid

2.7.7.2.4.6. Testpoint-to-Component Clearances

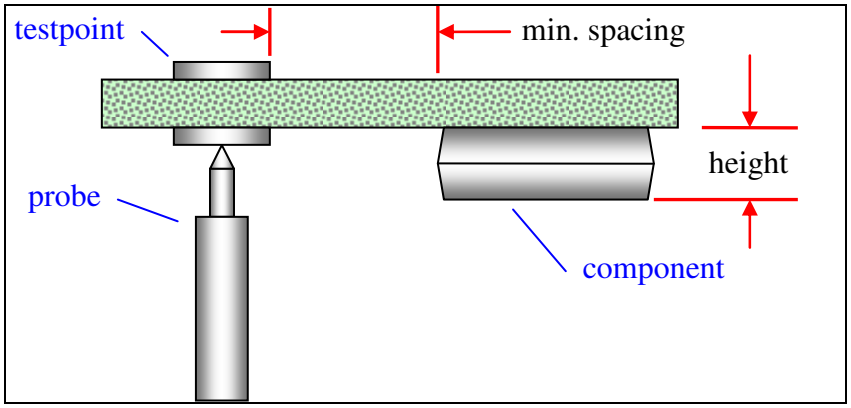


Figure 60: ICT Spacing

2.7.7.2.4.6.1. To prevent test probes from hitting adjacent components, and possibly breaking probes and components, a minimum center of testpoint to component body must be maintained per **Table 7** below:

Table 7: ICT Testpoint-to-Component Body Clearacnce Chart

Component Height	Minimum Spacing
0.000" - 0.125"	0.038"
0.126" - 0.250"	0.053"
> 0.251"	0.125"

2.7.7.2.4.6.2. Edge of testpoint to component lead shall be no less than .018".

2.7.7.2.4.6.3. Note 1: Component heights of >.250" should be avoided to prevent the need for expensive cut-outs in the fixture.

2.7.7.2.4.6.4. Note 2: No testpoints are to be placed within .200" of any board edge or tooling holes.

2.7.7.2.4.7. **Moving/Adding Testpoints—**Due to the extremely high cost of creating a test fixture, it is very important to keep the movement of testpoints and the addition of testpoints to a minimum when making ECO changes. The designer must keep an accurate ECO log file of all changes and additions (node name, testpoint reference designator, and X/Y location). When moving or adding a testpoint, keep a .100" clearance from existing testpoints and also from removed testpoints.

2.7.7.3. Flying Probe

2.7.7.3.1. Flying Probe testers test for many of the same manufacturing issues as ICT, but without the need of a “bed of nails” fixture. However, because of the nature of the test, it is used in low volume situations rather than high-volume. The board is clamped onto the tester along its two long edges and is then probed by way of four or more independent probing arms that are mounted at an angle. Although it can test for many of the same manufacturing

problems, such as solder opens, solder bridges, missing parts, wrong parts, reversed parts, and component values, it is not robust enough to check for defects (e.g., static damage) to logic components. Flying probe testing has become the preferred choice by many for its low cost, fast programming time, and ease in achieving 100% nodal access.

Table 8: Summary of Flying Probe Test Advantages and Disadvantages

Pros	Very cost effective Fast programming time (approx 2 days) Much easier to obtain 100% nodal access
Cons	Much slower to test individual boards (approx 40 minutes) than ICT Not able to test for as many problems as ICT

2.7.7.3.1.1. **Testpoint Side—**Same as ICT.

2.7.7.3.1.2. **Testpoint Size and Shape—**Standard testpoint size and shape is .020"-025" Round. Smaller sizes may be accommodated, but only by approval of the Test Engineer.

2.7.7.3.1.3. **Test Target Type—**Same as ICT.

2.7.7.3.1.4. **Testpoint-to-Testpoint Clearance—**Most significantly, flying probe testing does not require a minimum TP-to-TP clearance, other than to maintain the minimum standard fabrication pad-to-pad clearances.

2.7.7.3.1.5. Minimum Number of Testpoints, by Node Type

2.7.7.3.1.5.1. Signal Node = 1 (Same at ICT)

2.7.7.3.1.5.2. Power Node = 1

2.7.7.3.1.5.3. Ground Node = 10 (evenly distributed, with at least 1 in each corner of the board)

2.7.7.3.1.6. **Testpoint-to-Component Clearances—**In general, edge-of-testpoint-to-edge-of-component-lead distance can be the same as the minimum standard fab. pad-to-pad clearances. The table below shows minimum testpoint edge-to-component-body clearance rules:

Table 9: Flying Probe Testpoint-to-Component Body Clearance Chart

Component Height (with PCB)	Minimum Spacing
0.000" - 0.125"	0.038"
0.126" - 0.250"	0.053"
> 0.251"	0.125"

2.7.7.3.1.6.1. Note 1: No testpoints are to be placed within .200" of any board edge or tooling holes.

2.7.7.3.1.7. **Moving/Adding Testpoints—**Although a fixture is not involved in Flying Probe testing, it is still advisable and helpful that the designer keep an accurate ECO log file of all changes and additions (node name, testpoint reference designator, and X/Y location). This only applies if the number of changes is not excessive (that is, no more than a couple dozen).

2.7.8. Planes

2.7.8.1. Planes provide an efficient way to distribute power and ground throughout a design, while providing a return path for each signal. However, not all planes are single sheets of copper carrying only one power or ground. Some carry more than one voltage or ground signal—through the use of plane splits—for various reasons. It may be necessary to split planes in order to:

2.7.8.1.1. Keep noise under control
2.7.8.1.2. Provide for multiple voltages
2.7.8.1.3. Separate analog and digital circuits
2.7.8.1.4. Route power supplies in small, local areas
2.7.8.1.5. Provide an alternative to large high-current traces
2.7.8.1.6. Provide low impedance/low inductance signal path returns
2.7.8.1.7. Provide low resistance returns for power supplies
2.7.8.1.8. Use as a reference plane for impedance calculations

2.7.8.2. These plane shapes play a critical role in the performance and characteristics of a printed circuit board and, therefore, should be considered before routing a design.

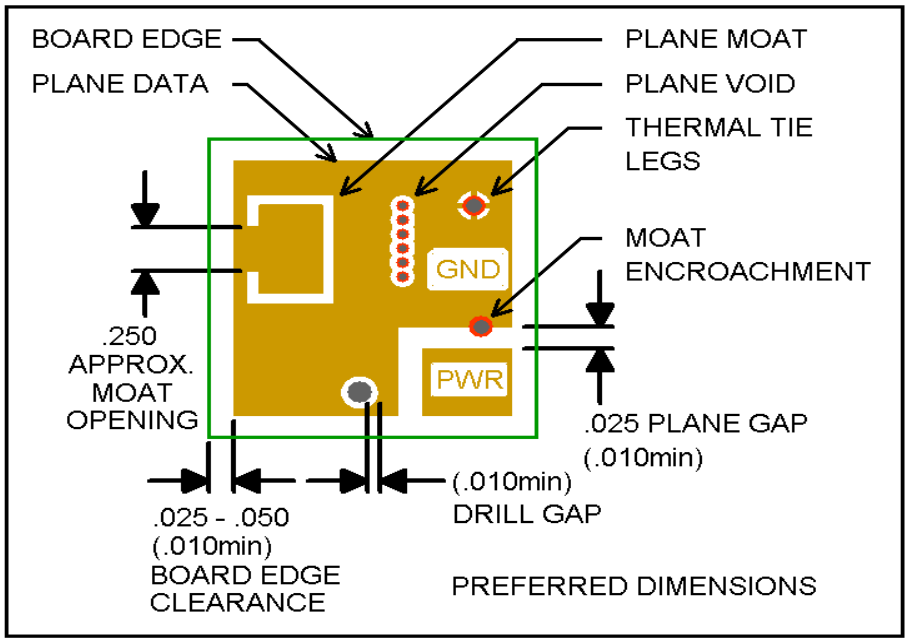


Figure 61: Plane Shape Definitions and Spacing Requirements

2.7.8.3. When plane shapes are being defined, a grid system of .025" (.005" min.) should be used to achieve the desired spacing requirements and to help maintain true shaped geometries. The definition and setup parameters of these plane shapes should meet the preferred spacing requirements shown in **Figure 61**. The copper balance between layers and the coupling of plane layers should both be considered when defining these plane shapes.

2.7.8.4. The connections being made to the planes must also be considered for thermal management to prevent any DFM issues. SMD and thru-hole part pads that tie directly to the plane shapes must use thermal tie legs to eliminate poor solder joints that would otherwise occur during the assembly process. If the plane connection to the part pad exceeds 80% of the pad geometry, then the plane will draw too much heat from the solder joint, creating a poor connection. (See **Figure**

62, and also refer to Library Padstack Definitions.) Vias should be buried in the plane (without thermal relief), since they do not require a solder connection.

2.7.8.4.1. Maximum Tie Leg Width = (Pad Size • 0.8)/# of Tie Legs

2.7.8.4.2. Web Clearance = .010" (for Pad Size < .060")
= .015" (for .060" <= Pad Size < .125")
= .025" (for Pad Size >= .125")

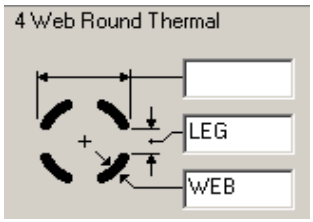


Figure 62: Thermal Relief Tie Leg Definitions

2.7.8.5. After the plane shapes have been defined and the routing has been completed, the designer should review all of the plane shapes for common errors. A review of the thermal tie legs should be done to ensure that a minimum of two tie legs have been achieved for each connection, and that any high current connections have increased tie legs to accommodate the current rating. The thermal relief should also be reviewed for overlapping thermals, and overlapping of plane clearances (see **Figure 63**).

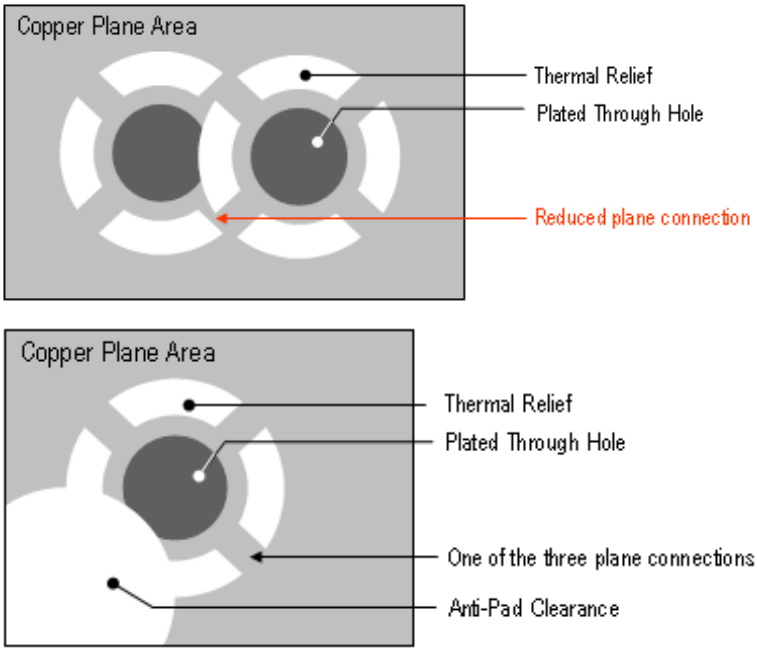


Figure 63: Thermal Tie Overlap

Courtesy of TTM Technologies

2.7.8.6. A visual inspection should also be performed, to locate and correct any improper plane gaps, moat encroachments, and plane voids created by pins or vias placed too closely together.

2.7.9. Critical / Interactive Routing

2.7.9.1. At this point, considering that all mechanical, placement, and routing stages have been accomplished, the designer can now either systematically route the entire board by hand (interactively) or hand route some of the critical aspects of the design and auto-route the rest. Signals that are commonly hand routed include: Analog/RF circuitry, high-current signals, off-board interface connector circuits, memory, and miscellaneous short routes.

2.7.9.2. Analog/RF Circuitry

2.7.9.2.1. On analog boards, placement is the more critical part of the design process. A good analog placement will almost certainly make the routing process a simple task of point-to-point connections with very short traces. See the section on Placement (p. 23) for a more detailed discussion of analog part placement. **Figure 64** shows an example of an analog circuit. The placement dictates that the trace routing will be very short and direct. During the placement and routing stages your attention should be given to maintaining isolation between the input and output flow of the circuitry.

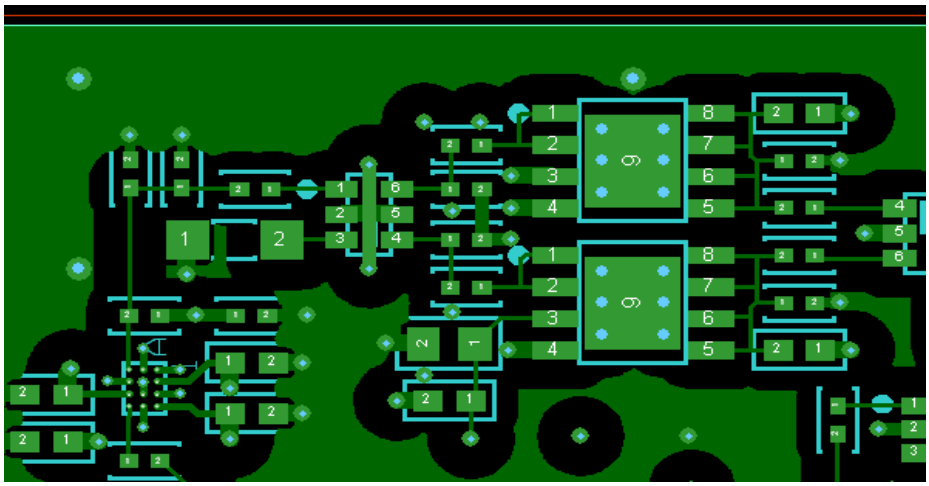


Figure 64: Analog Circuit to be Routed

2.7.9.2.2. In analog designs, it is preferred to use a slightly larger trace width of between 8Mils and 12Mils for signal routing. RF designs are often more sensitive to trace width variations, so, whenever possible, it is preferred to use a trace width equal to the pad width of component footprints. Additionally, some analog and RF circuits require impedance control, which can make trace width options difficult, so this should be considered early in the design process.

2.7.9.2.3. On analog and RF designs it is common to flood the surface layers with a ground fill, as shown in **Figure 64**. This is also sometimes done on selected areas of very high speed digital designs. Keeping track of this process is necessary because, if it is forgotten, then later when the flood is applied, there will likely be many unconnected islands instead of a continuous flood. This may be difficult to resolve if there is much internal layer routing under these areas, preventing the designer from adding the necessary vias to 'stitch' these unconnected islands to the relevant internal planes (usually GND). If these islands are not stitched to the relevant planes, then they are

not serving any useful purpose and can, in fact, cause crosstalk issues by providing a floating 'bridge' for electromagnetic coupling between signals.

2.7.9.3. High Current / High Voltage Routing

2.7.9.3.1. The design and layout of high voltage and high current applications are critical to the performance and safe handling of the PC board. High current designs will require either the use of wide traces or plane shapes to achieve connectivity as seen in **Figure 65**. The width of the trace is driven by the current (Amps) requirement of the signal path. Once current is determined, the Trace Current Capacity Chart (Appendix A) will help you to choose the appropriate trace width for your design. When necessary, the thermal ties to pads or the trace-width-to-pad-size ratio may have to be violated in order to meet your high current design requirements. The designer must consider the possible impact of this violation and seek the approval of the customer.

2.7.9.3.2. In high voltage applications special care should be given to the spacing of conductors. Refer to IPC-2221A, Table 61: Electrical Conductor Spacing for the appropriate spacing of conductors (included as Appendix B). It is important to think three-dimensionally when designing a high voltage circuit. The designer must not only consider the spacing of traces and plane shapes, but also the spacing of components, component leads, adjacent layers, mounting holes, chassis housing, and any other nearby conductor. The designer should also consult the engineer regarding any possible handling issues or necessary labeling for the high voltage circuitry.

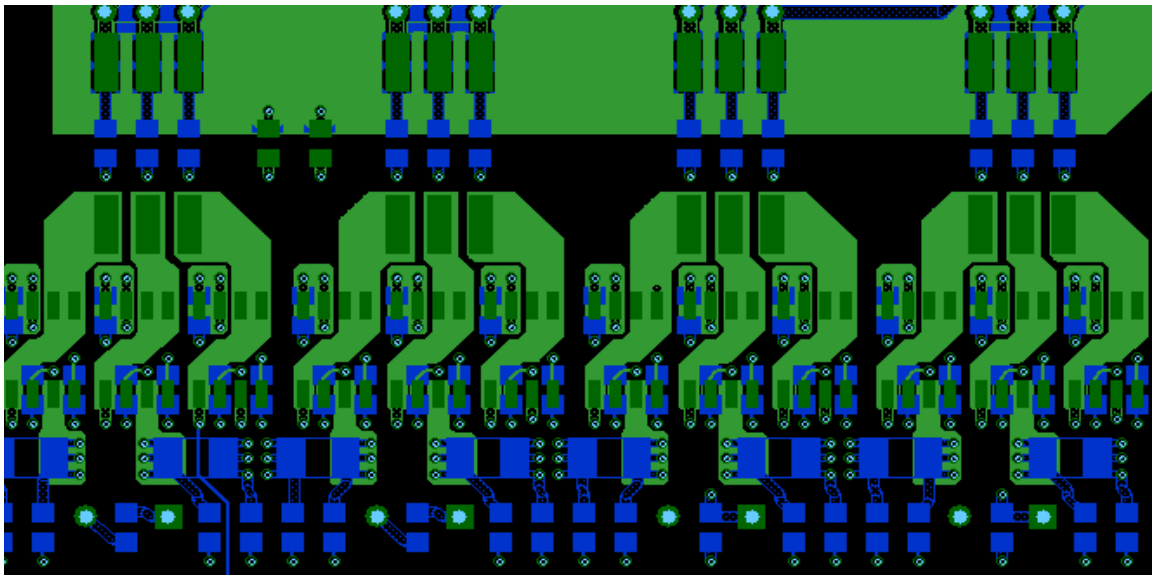


Figure 65: High-Current Traces

2.7.9.4. Route off-board connections

2.7.9.4.1. In this phase, routes to off-board connectors should be completed. This is relevant for those connections between the off-board connectors and any buffers, drivers, or terminating devices attached to them. Care needs to be taken here to make sure the impedances of traces are correct. Many engineers will specify 50-Ohm (common for digital signals) or 75-Ohm (for video and ECL signals) single-ended routes, or 100-Ohm differential traces.

2.7.9.4.2. Some connectors present an impedance of approximately 100 Ohms. This is particularly the case in many dual-row, IDC-type connectors used with ribbon cables. If high speed signals are to be routed to these connectors, then you should at least query the trace impedance with the engineer.

2.7.9.4.3. Another thing that appears quite commonly is that high density backplane connectors are often overcrowded with signal traces, and there are few, if any, ground pins amongst them. This shortage of ground pins will cause some serious signal integrity problems, as the ground return path will be a long way from the actual signal pins. There are a number of common methods of avoiding this problem.

2.7.9.4.4. First, most backplane connector systems are now available with 'shielded' connector versions. These have one or two extra rows of pins that are used for a metallic shield that is optionally mounted above or below the connector. This provides one or two ground pins for each column of signal pins.

2.7.9.4.5. A second method is to suggest that busses might be able to be multiplexed onto the backplane. Since each buffer/driver will present some delay to the signals, the possibility of multiplexing is dependant on system timing considerations. It is, however, an option that should be suggested to the engineer.

2.7.9.4.6. Lastly, there are many new connector types becoming available all the time. These are increasing in density and also becoming available in SMT technology for even higher pin counts. If the engineer uses these extra pins to increase the number of ground pins, instead of merely increasing the number of signals, then this will alleviate the signal integrity problem.

2.7.9.4.7. You also need to be aware of 'standard' interface specifications. For example, VME bus boards specify that the signals to/from the backplane connectors must be no more than two inches in length. Desktop PCI (**Figure 66**) specifies that the PCICLK signal going to the core logic interface device must be 2.5 inches long. This will be affected by placement, so make sure you are aware of these specifications before you commence the placement phase of the design. In addition to the VME and PCI specifications, other common standards of which you should either be aware or have available are:

2.7.9.4.7.1. PC104

2.7.9.4.7.2. PCMCIA

2.7.9.4.7.3. Front Panel Data Port (FPDP)

2.7.9.4.7.4. Futurebus[6]

2.7.9.4.7.5. PCI-Express

2.7.9.4.7.6. SATA

2.7.9.4.7.7. Infiniband[7]

2.7.9.4.7.8. USB

2.7.9.4.8. Other specifications may become necessary at any time.

[6] "Futurebus" is a Registered Trademark of Force Computers GMBH, Fed. Rep. of Germany

[7] "InfiniBand" is a Trademark/Servicemark of the InfiniBand Trade Association

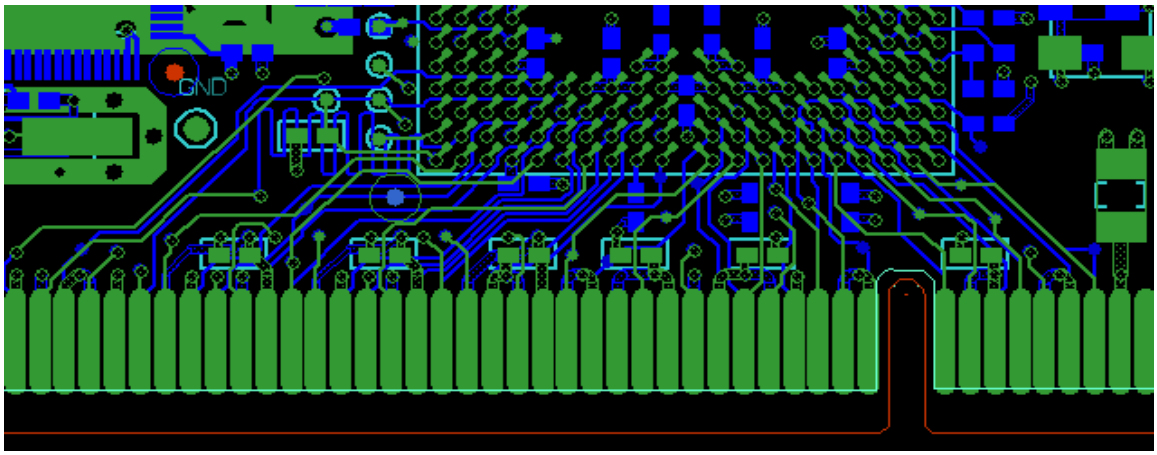


Figure 66: PCI Bus Routing

2.7.9.5. Memory

2.7.9.5.1. Memory devices are often hand routed to maintain a clean, organized pattern of routing. These devices should typically be routed in a daisy-chain fashion, which has been approved by the engineer. Special care should be taken during routing to maintain proper separation between address, data, and control signals associated with these devices. The routing constraints for these signals are also becoming more demanding. It is now common for memory requirements to include elements such as delayed and matched lengths, which often can be better planned and controlled with interactive routing. However, with proper setup, many times these same results can also be accomplished using the auto-router. See **Figure 67** for an example of memory routing.

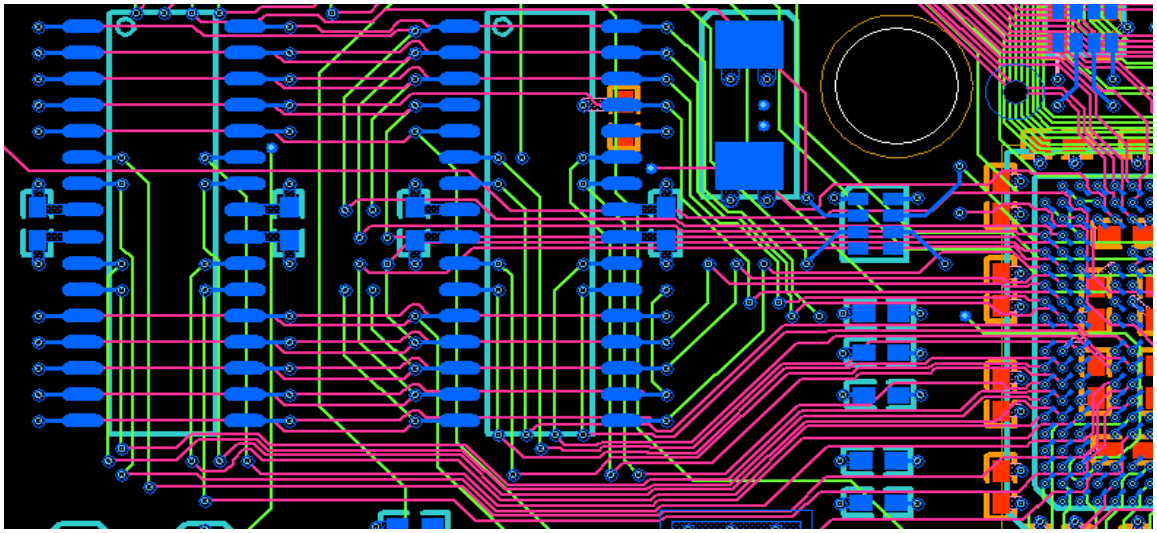


Figure 67: Memory Routing

2.7.9.6. Miscellaneous

2.7.9.6.1. There may be other critical nets or specified manufacturer guidelines that should be addressed before routing the remainder of the design. Anything that has a defined routing requirement should take priority, to ensure its

success. This may include layer-specific signals due to technology, impedance requirements, length constraints, or any signals that the engineer has determined to be critical to the performance of the design. These signals should be routed and approved by the engineer before proceeding to the next stage of the design.

2.7.10. Critical Route Review

2.7.10.1. If a board has critical signals, then the engineer in charge of the project must review and approve their routing before the rest of the signal trace routing can proceed. This review may be accomplished either by viewing the database with a browser, by looking at printed documents, or by reviewing the design on the designer's CAD station. In any event, the engineer must give clear approval before work can go forward. Changes may be specified clearly enough that no further review is necessary, but changes that are in any way ambiguous or unclear should be reviewed again before routing continues.

2.7.11. Auto-Routing

2.7.11.1. Auto-routing software is capable of completing very dense high-speed designs while reducing the design-to-fabrication time of boards. Proper set up of the design before proceeding with the auto-router plays a critical role in achieving desirable results. The auto-router setup is now the designer's primary tool for controlling not only how the auto-router will behave, but also the amount of clean-up that will be needed, and how much manual interaction will be required to complete the final connectivity of the design. Because the setup stage is so important, *do not be in a hurry to push the button.*

2.7.11.2. In fact, before a designer even considers opening up the auto-router setup screen, certain tasks should have already been completed. These tasks include:

2.7.11.2.1. Add obstructs for mechanical items (e.g., mounting holes, fiducials, hardware, etc.)

2.7.11.2.2. Assign net rules, clearances, layer restrictions, and grid systems.

2.7.11.2.3. Define all route obstructs (via and/or trace keepouts; these may be layer specific).

2.7.11.2.4. Isolate specific circuit areas (RF, digital, analog circuit separation).

2.7.11.2.5. Verify that all SMD pads have a fanout via.

2.7.11.2.6. Manually route all critical circuits, manufacturer suggested layouts, and then protect critical traces.

2.7.11.2.7. Add obstructs for plane splits (so no signals cross splits or they cross in a defined area.) See **Figure 68**.

2.7.11.2.8. Save a backup copy of the design (to revert back to if the results of the AR are not acceptable)

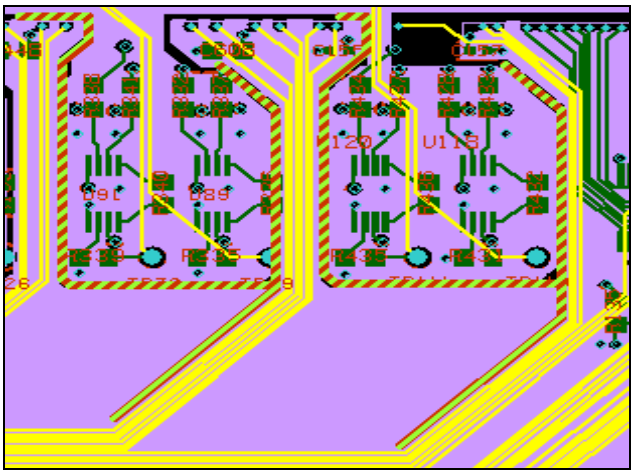


Figure 68: Route Obstructs to Prevent Crossing a Plane Split

2.7.11.3. Auto-Router Setup Stages

2.7.11.3.1. After the above items have been addressed, we are ready to set up the auto-router. You should be prepared to run several incremental passes using the auto-router, rather than expecting one comprehensive pass to route the entire board. Each pass will be set up to route different aspects of the design. Defining and limiting the auto-router to route either small groups of related nets, or particular areas of the design, will help you control the priority and quality of the overall routing task.

2.7.11.3.2. You should break down the nets into classified groups to allow for controlled priority routing. Listed are some common groups of signals that can be found in most designs:

- 2.7.11.3.2.1. Critical nets: (if not manually routed)
  - 2.7.11.3.2.1.1. Clocks
  - 2.7.11.3.2.1.2. Differential pairs
  - 2.7.11.3.2.1.3. Nets with Delay/Matched lengths
- 2.7.11.3.2.2. Busses:
  - 2.7.11.3.2.2.1. Address
  - 2.7.11.3.2.2.2. Data
  - 2.7.11.3.2.2.3. Input
  - 2.7.11.3.2.2.4. Output
- 2.7.11.3.2.3. Default:
  - 2.7.11.3.2.3.1. All non-priority signals

2.7.11.3.3. These groups may now be auto-routed individually in progressive stages. It is now the designer's job to consider any routing challenges that can be improved by the sequence in which they are completed. Through changing routing parameters and priority, a variety of different results can be achieved. The figure below is an example of a common progression of routing stages a designer might use in the auto-router for achieving connectivity.

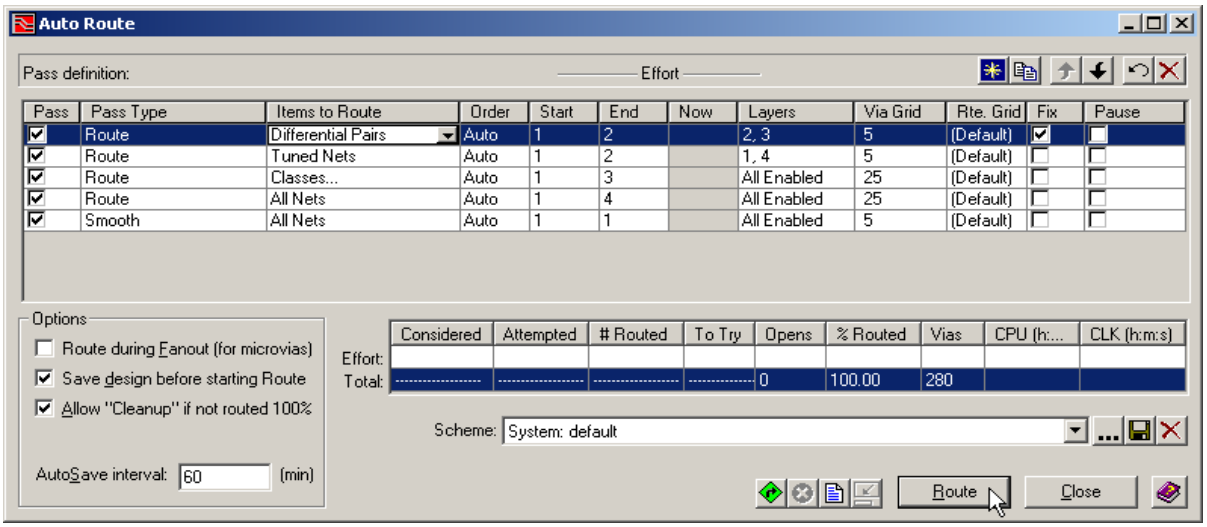


Figure 69: Routing Stages

2.7.11.3.3.1. First Stage

2.7.11.3.3.1.1. Critical nets:

2.7.11.3.3.1.1.1. -Clocks

2.7.11.3.3.1.1.2. -Differential pairs

2.7.11.3.3.1.2. Fix or lock the nets after reviewing/modifying

2.7.11.3.3.2. Second Stage

2.7.11.3.3.2.1. Critical nets:

2.7.11.3.3.2.1.1. -Nets with Delay formulas

2.7.11.3.3.2.1.2. -Nets with Matched lengths

2.7.11.3.3.2.2. Fix or lock the nets after reviewing/modifying

2.7.11.3.3.2.2.1. High Density Areas (BGAs, etc.)

2.7.11.3.3.3. Third Stage

2.7.11.3.3.3.1.1. Busses:

2.7.11.3.3.3.1.1.1. -Address

2.7.11.3.3.3.1.1.2. -Data

2.7.11.3.3.3.1.1.3. -Input

2.7.11.3.3.3.1.1.4. -Output

2.7.11.3.3.4. Fourth Stage

2.7.11.3.3.4.1.1. Default:

2.7.11.3.3.4.1.1.1. -All non-priority signals

2.7.11.3.3.5. Fifth Stage

2.7.11.3.3.5.1.1. Clean Up Pass:

2.7.11.3.3.5.1.1.1. -All unlocked signals

2.7.11.3.4. The stages above may require more passes than just the individual ones shown. The auto-router may also fail to achieve 100% connectivity with a

particular design. Therefore, it may be necessary to either change the sequencing or regions of the design that are the first to be routed, to add more layers to the layer stack-up, or to complete connectivity by manually routing the remaining open connections. Also, by using route obstructs, the auto-router can be forced to route in specific paths. Although this method can seem somewhat time consuming, it is still much faster than manual routing.

2.7.11.4. Cleanup

2.7.11.4.1. The designer should review each layer individually, as well as all layers collectively, to look for obvious areas of the routing that can be cleaned up. Do this by setting a manageable view window, and pan across the board, layer by layer. The auto-router often leaves unnecessary bends and “wrap-around” traces, especially in the areas of the BGAs. See **Figure 70**.

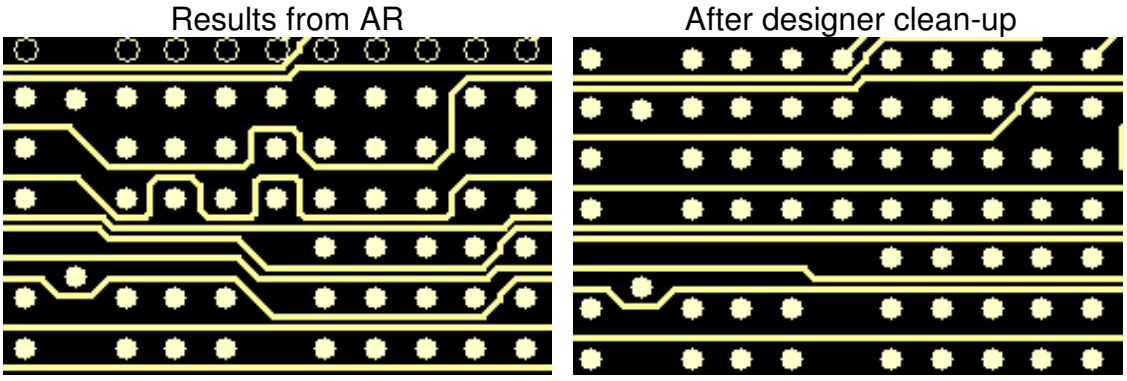


Figure 70: Trace Cleanup

2.7.11.5. Review Reports

2.7.11.5.1. A trace length report should be generated and reviewed. Usually excessive lengths can be shortened considerably. These excessively long traces primarily occur in dense designs, and are some of the last traces placed by the auto-router. By reviewing the routes in their entirety (all trace layers), they can often be easily shortened. See the example below.

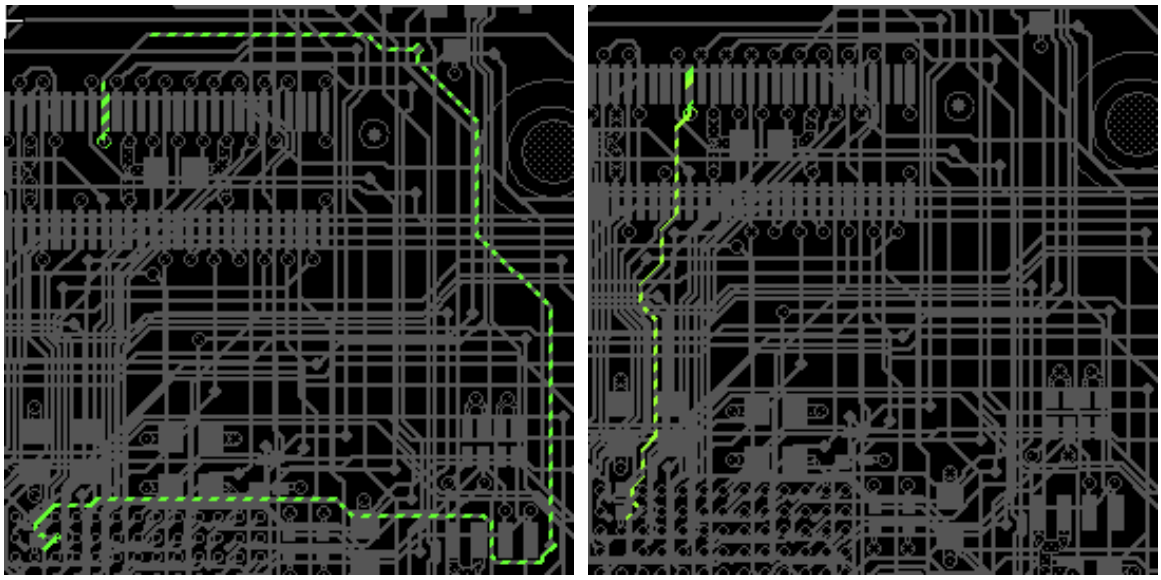


Figure 71: Shortening Unnecessarily Long Traces

2.7.12. Miscellaneous Items

2.7.12.1. There are often additional items or features specific to a design that a customer might request to be included on their board. Some items are more common than others, but each must be considered with every design. These may include some of the following items.

2.7.12.2. Etched Text

2.7.12.2.1. It is common practice to include the fabrication and revision number in etch on the bottom side of the board. Customers may also request additional information such as logos, labels, or other part numbers to be included on the top or bottom side of the design.

Figure 72: Etch Markings

2.7.12.2.2. Caution should be taken when placing these items onto the board to prevent common errors. Check to make sure that the etched items are not placed over traces, vias, pads, or any other electrical features on the board.

Also be sure not to place any silkscreen information over the etched text during clean up.

2.7.12.3. Layer Window

2.7.12.3.1. Layer windows are often included in designs to ensure that the layers were stacked correctly during the fabrication process. ODA currently uses two methods for creating layer windows:

2.7.12.3.1.1. Sequential text on all etch layers (see **Figure 73**)

2.7.12.3.1.2. Copper areas along one edge of the board (see **Figure 74**)

Figure 73: Layer Etch Markings

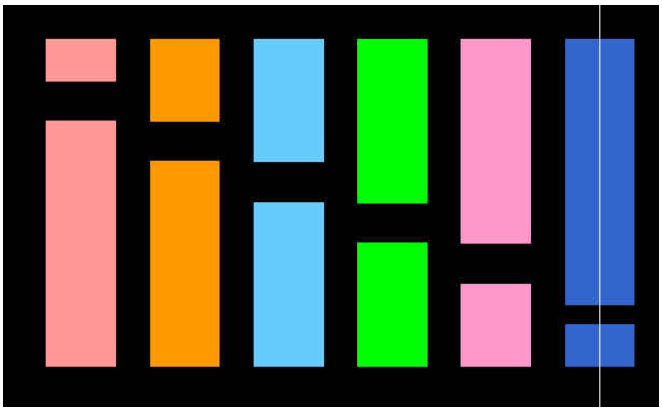


Figure 74: Copper Shapes Placed on an Edge of the Board

2.7.13. Miscellaneous Trace DFM Issues

2.7.13.1. Below are a few examples of miscellaneous trace and pad issues which should be considered. These issues can affect assembly and long-term reliability, even after the PCB is in the field. Designers should avoid these throughout the whole design process because most issues are easier to correct when they are created, instead of waiting until the DRC stage, when many more design elements may be affected.

2.7.13.2. Trace Entry into Pad

2.7.13.2.1. Lands may be approached by their connecting traces on any of the four sides as well as from the corners of the pad (see **Figure 75**).

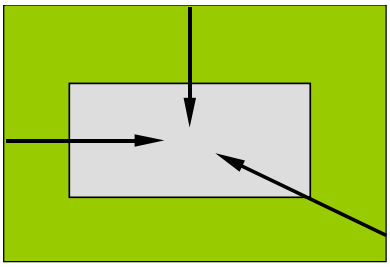


Figure 75: Trace Entry into Land Pads

2.7.13.2.2. It is permissible for a trace to overlap the edge of a connecting land and then turn into the center, provided the trace does not extend more than 80% of the length of the pad. **Figure 76-A** shows an acceptable trace that does this. It is not permissible for a trace to run parallel to a connecting land with a gap of <5 mil. Doing so creates a niche in which acid collects during the etching process, thus causing problems with the board over the long term. **Figure 76-B** illustrates what to avoid.

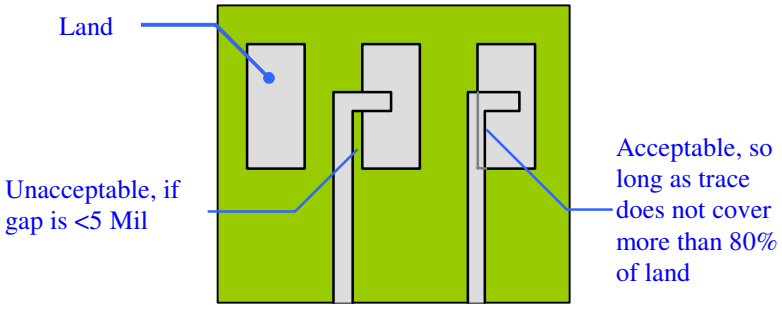


Figure 76: Trace/Land Overlap

2.7.13.2.3. Trace widths, as they enter a land, should normally be no wider than 80% of the width of the land. This is in order to keep extra heat from being pulled away from the land during the assembly operation. One possible exception to this rule would be current-carrying lands. The customer may request that these types of lands have their associated trace widths up to 100% of the land width.

2.7.13.3. Trace Angles

2.7.13.3.1. Traces should be routed using 45° or 90° angles. Signals should not have any odd angles along their length, and any angles greater than 90° (also known as "*critical angles*") must be corrected. In **Figure 77** the critical angle is fixed by replacing it with a combination of 45° traces.

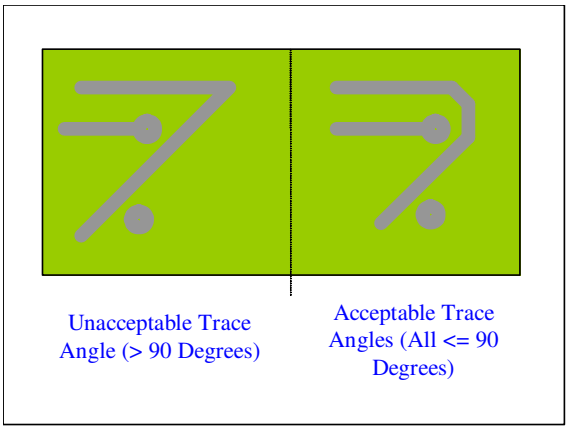


Figure 77: Trace Angle Example

2.7.13.4. Vias Under Components

2.7.13.4.1. Avoid placing vias underneath discrete chip components (e.g., 1206, 0805), when possible. Vias under chip components can cause the part to skew when wave soldered, making a poor connection.

2.7.13.5. Adjacent Fine Pitch Land Routing

2.7.13.5.1. Adjacent lands that are to be connected should have the trace enter and exit the land from the "toes" instead of more directly from the sides of the lands. See **Figure 78**. This method of routing adjacent lands will greatly aid in the assembly inspection process, since it will be clear that there is no unintentional solder bridging between the two pads.

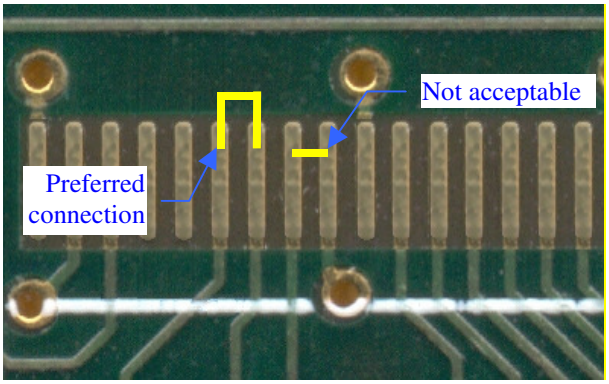


Figure 78: Preferred Connection of Fine Pitch Parts

2.8. DRC (Design Rules Checking)

2.8.1. The DRC process will aid in determining if the layout meets the design requirements, and if it is ready for output processing. DRC will compare lists of rules to the data in a design and output error reports. Most times this report can be viewed graphically for easier clarity.

2.8.2. Become familiar with which items are checked by your CAD system's DRC, and which types of problems are not checked. Bear in mind that the DRC tool is only an aid to meeting the design requirements, and that it cannot guarantee an error-free layout.

2.8.3. There are two types of DRC processes in most CAD tools: Online (or Dynamic) DRC, and Batch DRC.

2.8.4. Online (Dynamic) DRC

2.8.4.1. Online DRC evaluates each change made in the design to make sure that no rules are violated, *while the changes are being made.* Any changes that violate the rules are not implemented.

2.8.4.2. Online DRC rules may be changed at any time during the design of a PCB. However, only current changes are checked against the rules, so if previous changes violate the current rule, they will not be detected by online DRC.

2.8.4.3. Online rules typically verify the following items:

2.8.4.3.1. Components—Parts and their Rotation

2.8.4.3.2. Opens—Fanouts and Nets

2.8.4.3.3. Traces—Widths, Pad entry and Restricted layers

2.8.4.3.4. Via—Size and maximum count

2.8.4.3.5. Grids—Via and Traces

2.8.4.3.6. Lengths—Maximum, Minimum, Matched, Delay lengths and Stubs

2.8.4.3.7. Differential Pair—Length Matching and Delays

2.8.4.3.8. Crosstalk—Parallelism and estimated crosstalk

2.8.4.4. The online DRC function may be disabled, but is usually left turned on, except under unusual circumstances.

2.8.5. Batch DRC

2.8.5.1. A batch DRC is only executed at the request of the designer. Usually, a batch DRC is performed toward the end of the design cycle, when the designer is wrapping up the job.

2.8.5.2. Rules are entered through a matrix, then the DRC is run, producing a (sometimes) lengthy report. Changes that are made to the design do not instantly alter errors being reported, and errors that are actually corrected will not appear as corrected until the next time batch DRC is executed.

2.8.5.3. Batch rules typically verify the following items:

2.8.5.3.1. Proximity—spatial checking of elements to elements

2.8.5.3.2. Hangers—trace stubs not required for connectivity

2.8.5.3.3. Trace Loops

2.8.5.3.4. Plane Violations—check for connectivity and proper pour

2.8.5.3.5. Dangling Vias/Jumpers—vias and jumpers not part of connectivity path

2.8.5.3.6. Unplated connected pins

2.8.5.3.7. Vias and test points under parts

2.8.5.3.8. Minimum Annular Ring

2.8.5.3.9. Missing Pads—on soldermask, pastemask, and conductive layers

2.8.5.4. Even though the batch DRC process is simple and straightforward, achieving a passing design can get complicated. After DRC has run, errors may demand correction. These errors may be simple or complicated to fix, requiring few or many design changes to satisfy the rules. Afterwards, if the designer feels the rules are satisfied, another DRC check must be run to verify that the errors are

actually now corrected, and if there are no new errors. This process is repeated until the batch DRC checks are satisfactory.

2.8.5.5. What is meant by “satisfactory?” The DRC may identify items as errors that really are not errors. These “bogus” errors may be disregarded. Other flagged items may indeed violate a rule that has been entered, but for some other reason may still be acceptable. For any items that remain flagged as errors, the designer should know why the error has been discounted, and be able to explain that decision, if questions should arise.

2.8.6. ODA Project Checklist (Routing and Planes)

2.8.6.1. At this point all items in the Routing and Planes category within the ODA Project Checklist spreadsheet should be marked off (*marked off* means done or considered).

2.9. Wrap-Up

2.9.1. At this point the design should already be completely routed and submitted to the engineer for final route review. Some final processing and clean up of the design will be necessary for creating proper output data and documentation that can be used for fabricating, manufacturing, testing, and troubleshooting the design. Following the wrap-up procedures and paying close attention to detail is mandatory, since it is this information that determines how the board will be built.

2.9.2. Below is the typical ODA process for wrapping up a design:

2.9.2.1.	**Renumber**	Renumber reference designators; create WAS/IS list
2.9.2.2.	**Silkscreen**	Clean up text orientation and position; Add customer information and board numbers
2.9.2.3.	**Film Common**	Update title block; Verify layer names match fabrication stack-up
2.9.2.4.	**Fabrication Drawing**	Dimension all board features; Define layer stack-up; Create drill chart; Update notes and title block information
2.9.2.5.	**Assembly Drawing**	Clean up text orientation and position; Add notes or instructions; Update title block
2.9.2.6.	**Final Review**	Send database to customer for final review; Once approved, generate outputs
2.9.2.7.	**Generate Output Data**	Create deliverable files: Gerbers, NC Drill, Netlist, X/Y list, Fiducial list, Testpoint list, Drawing formats, Read.me
2.9.2.8.	**Valor DFM Check**	Verify output files for manufacturing issues (Gerbers, Netlist, NC Drill)
2.9.2.9.	**Archive**	Clean-up database; Send database and deliverable outputs to customer; Move database to archive directory

2.9.3. Details on each of these steps are given in the sections below.

2.9.4. Renumber

2.9.4.1. The renumbering of reference designators helps organize the labeling of the components on a board so that they are easy to locate when assembling and troubleshooting. The common practice is to sequentially reorganize the reference designators from left to right, top to bottom, in appropriate bandwidths, depending upon the size and shape of the design. This is the preferred method for standard ODA practice, but may vary with each customer.

2.9.4.2. It is extremely important to maintain documentation of this renumbering, typically known as a "WAS/IS" list. This information relates the old reference designator to the new reference designator, and is necessary for back annotating the changes into the schematic. With some designs, the schematic is linked to the design database, so that the back annotation automatically occurs. However, this document – the WAS/IS list – should still be maintained, because it is still valuable in relating old reference designators that might appear in some of the supporting documentation and design guidelines.

2.9.5. Silkscreen

2.9.5.1. The silkscreen is a helpful tool in identifying components on the board. It should have a consistent flow that allows for easy identification of parts while using a minimum of leaders in difficult areas. Special care should be taken to ensure that each device has its appropriate associated markings, such as polarity, pin #1 location, 10th pin marker for fine pitch parts, or connector pinouts. Some parts may require additional labeling that should be specified by the customer. This may include labeling connectors, LEDs, switches, high voltage areas, or critical circuits (see **Figure 79**).

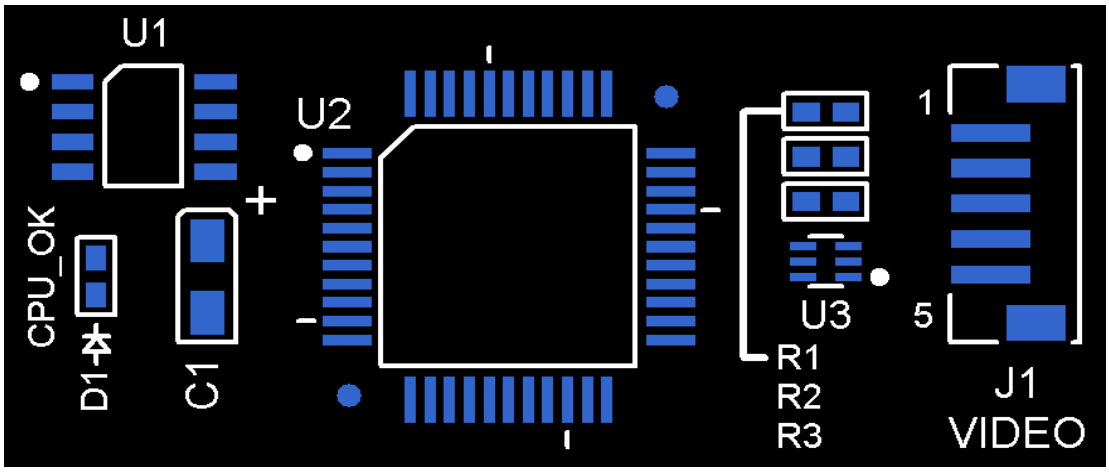


Figure 79: Silkscreen Markings and Clean-Up

2.9.5.2. Text on each board design should be clear and consistent. Letters must not cover surface-mounted land pads, nor should they overlap other text or silkscreen outlines. Some common mistakes to be avoided during cleanup include placing silkscreen text over etched text, on top of fiducials which include an enlarged soldermask opening, and any cutouts or milled areas. It is also best practice to view the Soldermask layer when cleaning up the Silkscreen, so as to avoid these common mistakes.

2.9.5.3. Only two text rotations are allowed on the board: 0° and 90° (unless otherwise specified). Table 10: Text Size/Rotation shows standard sizes, spacing and styles for text.

Table 10: Text Size/Rotation

Type	Pref. Size	Minimum Size	Rotation	Line Weight
Ref. Des. (Screened – Standard)	.040"	.035"	0° or 90°	4
Ref. Des. (LPI – Advanced)	.035"	.025"	0° or 90°	3
Customer Silkscreen Info.	.100"	.075"	0° or 90°	6
Title Block Dwg. D-Size	.125"	.075"	0°	6
Title Block Dwg. B-Size	.075"	.050"	0°	6

2.9.6. Film Common

2.9.6.1. The title block should appear on each Gerber layer identifying the customer, board name, board number, revision, layer identification, date, and the associated ODA job number. This information should be updated appropriately with each revision and checked to ensure the layer names match the layer stack-up detail on the fabrication drawing. See **Figure 80**.

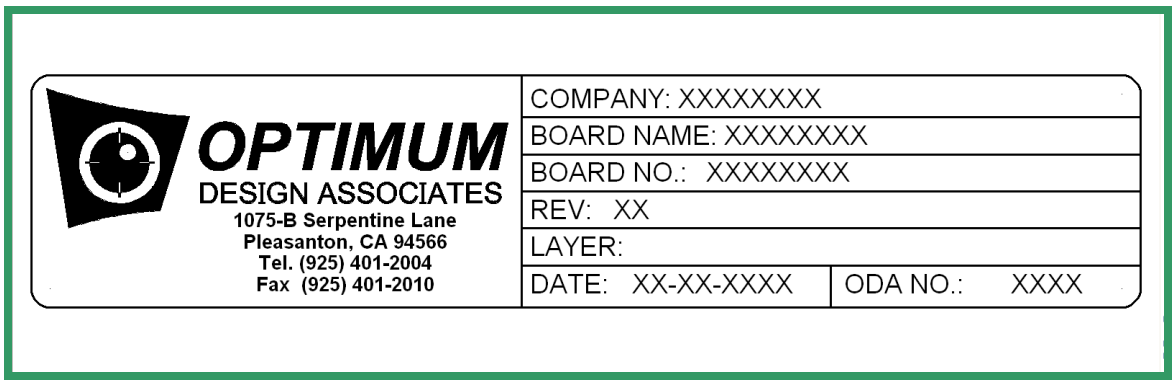


Figure 80: ODA Title Block

2.9.7. Fabrication Drawing

2.9.7.1. A fabrication drawing specifies how the PCB is to be manufactured. Appendix H contains a reproduction of a typical fabrication drawing containing all of the types of information that are described in the paragraphs that follow.

2.9.7.2. There are four major sections to a fabrication drawing—Board Illustration, Drill Chart, Section A-A, and Notes:

2.9.7.2.1. **Board Illustration** The board illustration shows the actual board outline with all cutouts, corners and radii. Usually only the top side of the board is shown. Board dimensions are referenced from the 0-0 point. The 0-0 point on the fabrication drawing must match the 0-0 point on the NC Drill data that were generated earlier in the Final Extract process. All drilled holes are indicated with symbols linking them to the drill chart.

2.9.7.2.2. **Drill Chart** Under a column labeled, “Symbol,” the drill chart lists each drill symbol used in the board

illustration. Other columns give further information regarding each hole type. The additional information is listed under columns labeled, “Diameter (in),” “Tolerance (in),” “Plated,” and “Quantity.” The hole size is the actual finished hole size after plating. The description of the hole plating is either “Yes” or “No.” The quantity is the actual number of holes drilled to this specification.

2.9.7.2.3. **Section A-A** The third section of the fabrication drawing is a view of the cross-section of the board, commonly referred to as a ‘sandwich.’ Items identified in this view are the overall board thickness, the layer numbers of the board, description of the layer (e.g., component side, VCC plane, etc.), dielectric thicknesses, and impedance information. If a Section A-A diagram is shown, as is usually the case, the board illustration must contain an indication of the point from where this view is seen.

2.9.7.2.4. **Notes** The last typical section on the fabrication drawing is the section containing fab. notes. While highly standardized, there is always some item to modify for the particular board on which you are working (e.g., finish type, gold fingers, or miscellaneous silkscreen aspects).

2.9.7.3. The fabrication drawing title block should also be filled out with the name of the customer, the name of the board, any drawing or fabrication numbers specified by the customer, and the ODA job number.

2.9.8. Assembly Drawing

2.9.8.1. An assembly drawing illustrates the location of components and any necessary instructions needed to complete the proper assembling of the board. As with the silkscreen reference designator clean-up, the assembly text must be also be cleaned up, with the exception that the reference designator text may be placed within the body of the part outlines for easier identification.

2.9.8.2. Each part location should be clearly identified on the drawing with notes to support any special procedures that may be required for installation. It may be necessary to include additional illustrations of detailed areas, profiles, or other views, if they help clarify how to assemble the board. This may include items such as board stiffeners, standoffs, card ejectors, conformal coating, or rework instructions.

2.9.8.3. The assembly drawing title block should also be filled out with the name of the customer, the name of the board, any drawing or assembly numbers specified by the customer, and the ODA job number.

2.9.9. Final Review

2.9.9.1. Final review is an opportunity for customer to make any last-minute changes or adjustments before the work is considered complete. Final review is done after all DRC checks have been completed and all drawings have the appropriate information.

2.9.9.2. Reviews are usually accomplished when the designer sends the customer the design database by either e-mail or by the file transfer protocol (FTP) over the Internet. The format of the database must match whichever reviewing tool the customer has available. This can be a Gerber file viewer (in which case Gerber output must be sent), or a free browser distributed by the CAD software developer (in which case the native database is sent), or some other tool. After review, the customer must send any instructions for changes back to the designer, usually by phone, e-mail message, or FAX. Written communication is preferable, for the obvious reasons.

2.9.9.3. Some engineers either have no review tools for the CAD data or Gerber output files, and therefore, must have the data sent in an alternative form. Since the Adobe Acrobat PDF Reader is widely available for free, some customers want their review data sent in .PDF format. Depending on the CAD tool, the .PDFs can be generated directly from their 'file/print' menu, or must first be generated in Gerber format, and then converted to .PDF format. Any changes must be sent to the designer in the same way as the first review method.

2.9.9.4. On rare occasion a customer will want an on-site review of their data. Since they are not usually familiar with the specific CAD tool used to design their boards, the designer is usually required to show the engineer whatever it is that they want to review. Although time-consuming and costly, some engineers find comfort in this review method. It also has the added advantage of instant feedback to the designer about any changes the engineer wishes to make. They can see and approve changes as they are made, with no room for confusion or misinterpretation of their instructions.

2.9.9.5. Once all changes have been made to the customer's satisfaction, authorization to proceed must be granted, which authorizes the designer to generate final output data.

2.9.10. Generate Output Data

2.9.10.1. After all DRC errors have been corrected and final approval has been obtained, it is time to generate final output data – the deliverables. Below is a general list of ODA standard outputs. This list is a minimum requirement, applicable to most design jobs. Actual outputs may vary from job to job, and per customer requirements.

2.9.10.2. Note: After Gerber files have been generated, it is important to review the output in an editor tool before proceeding to create the various .ZIP files.

2.9.10.3. Standard Output Files (Trace, Screen & Mask)

Filename	Source	Comment	Example(s)
<*Job_No*>*****.GDO**	CAD	Gerber files are reviewed in Gerber viewer.	2798TOP.GDO 2798IN01.GDO 2798IN12.GDO 2798BOT.GDO 2798SST.GDO 2798SSB.GDO 2798SMT.GDO 2798SMB.GDO

Note: *** are replaced by individual file names, jobs may contain many files.

2.9.10.4. Standard Output Files (Drill)

Filename	Source	Comment	Example(s)
<*Job_No*>*****.DRL**	CAD	Drill files containing location and size information for the NC drilling process [P=Plated; NP=Non-Plated; CNP=Contour Non-Plated]	2798P.DRL 2798NP.DRL 2798CNP.DRL

Note: *** are replaced by individual file names, jobs may contain many files.

2.9.10.5. Standard Output Files (Miscellaneous)

Filename	Source	Comment	Example(s)
<*Job_No*>**IPC.356**	CAD	IPC-D-356 standard netlist	2798IPC.356
<*Job_No*>**XY.LST**	CAD	List of all parts, name, rotation and their coordinates	2798XY.LST
<*Job_No*>**FID.LST**	CAD	List of all fiducials and their coordinates	2798FID.LST
<*Job_No*>**TP.LST**	CAD	List of all ICT test locations and their coordinates	2798TP.LST
<*Job_No*>**FAB.DXF**	Gerber viewer	DXF format plots of fabrication drawing	2798FAB.DXF
<*Job_No*>**AST.DXF**	Gerber viewer	DXF format plots of assembly top drawing	2798AST.DXF
<*Job_No*>**ASB.DXF**	Gerber viewer	DXF format plots of assembly bottom drawing NOTE: Make sure Gerber data is mirrored before generating	2798ASB.DXF
<*Job_No*>**READ.ME**	Microsoft Word	Verify all data is filled correctly i.e. date, customer, job numbers, board name, included files, etc.	2798READ.ME

2.9.10.6. Using the matrix below, create zipped archives (.ZIP) with the appropriate files as indicated. The matrix below is a general list of ODA standard outputs. Actual outputs may vary per job and customer requirements.

Table 11: Matrix of Deliverables

	Contents		
Deliverable Set	**Trace/Screen/Mask**	**Drill**	**Miscellaneous**
<*Job_No*>**Fab.ZIP**	<*Job_No*>**TOP.GDO** <*Job_No*>**IN*.GDO** <*Job_No*>**BOT.GDO** <*Job_No*>**SMT.GDO** <*Job_No*>**SMB.GDO** <*Job_No*>**SST.GDO** <*Job_No*>**SSB.GDO**	<*Job_No*>**P.DRL** <*Job_No*>**NP.DRL** <*Job_No*>***.DRL**	<*Job_No*>**READ.ME** <*Job_No*>**IPC.356** <*Job_No*>**FAB.PDF**
<*Job_No*>**Assy.ZIP**	<*Job_No*>**AST.GDO** <*Job_No*>**ASB.GDO** <*Job_No*>**SPT.GDO** <*Job_No*>**SPB.GDO**		<*Job_No*>**READ.ME** <*Job_No*>**IPC.356** <*Job_No*>**GEN.CAD** <*Job_No*>**FAB.MST** <*Job_No*>**XY.LST** <*Job_No*>**FID.LST** <*Job_No*>**TP.LST** <*Job_No*>**AST.PDF** <*Job_No*>**ASB.PDF**
<*Job_No*>**DXF.ZIP**			<*Job_No*>**FAB.DXF** <*Job_No*>**AST.DXF** <*Job_No*>**ASB.DXF**

Replace "***<Job_No>***" with the ODA-assigned job number.

2.9.11. DFM Verification (Valor)

2.9.11.1. In addition to the CAD system's DRC, all designs are checked by a third-party DFM (Design for manufacturing) verifier. The current DFM software is the Valor Trilogy package. Valor verifies the actual output data files for manufacturability.

2.9.11.2. Valor DFM should be done after the design has been checked with CAD verification and only needs validating before the job is handed off to be manufactured.

2.9.11.3. The files that are necessary for the Valor check include:

2.9.11.3.1. Completed Valor Verification Request Form

2.9.11.3.2. Trace-layer Gerbers

2.9.11.3.3. Mask and Screen Layers

2.9.11.3.4. NC Drill files

2.9.11.3.5. IPC-D-356 list

2.9.11.4. In addition, you need to specify the minimum gap to test for, report any intentional shorts or opens, and list any other special design features that may cause a false error to be reported by Valor.

2.9.11.5. The Valor checker will test the board using the parameters that are appropriate to your board's technology. You will receive a report of any items that indicate problem areas. The Valor checker does not approve or reject the design, but merely points out areas of concern that you, as the designer, must consider and decide a course of action. If items are found in Valor that you need to correct,

then, the design must be reworked, then verified with the native CAD DRC tools, and then new output files (deliverables) must be generated and (usually) resubmitted for another Valor check.

2.9.11.6. The feedback provided by the DFM process is invaluable to the designer, not only for the present design, but also for all future work. Use the Valor feedback to improve your skills as a designer, and to suggest modifications to processes and procedures that will protect against the identified errors showing up again in new designs.

2.9.12. ODA Project Checklist (Wrap-Up)

2.9.12.1. At this point, all Wrap-Up items within the ODA Project Checklist spreadsheet should be marked off (marked off means done or considered). And although many designers may have at one time worked on the job, it is now the responsibility of the designer that is wrapping up the project to ensure that all items on the Checklist are accounted for and checked off (☑). Don't just check off a box merely for the sake of checking it off. Truly consider each item that is unchecked, and make the appropriate decision.

2.10. Create Job Database Archive

2.10.1. Job archives are to be as small and compact as possible, but without losing any data. Files that are unnecessary, such as temporary work and log files, can take a lot of excess storage space, and should be deleted.

2.10.2. After directories are compacted, move final archive folder to the "Jobs for archive" directory on the ODA server. Folders here will be stored and backed and stored at multiple physical locations. Many times these folders have been reviewed and recalled at later dates for customer edits, ECOs and redesigns.

2.10.3. ODA Project Checklist (Shipped)

2.10.3.1. At this point, all Shipped items within the ODA Project Checklist spreadsheet should be marked off (marked off means done or considered).

This completes Part I of the Design Book. The material just presented describes the standards in the context of the work flow of a project.

Part II is Special Topics, and includes Cad-Specific Procedures, and High Speed Design Rules.

Part III is a collection of useful information for designers to use as reference material. This material will be most helpful when answering questions that arise during the course of designing a PCB at Optimum Design Associates.

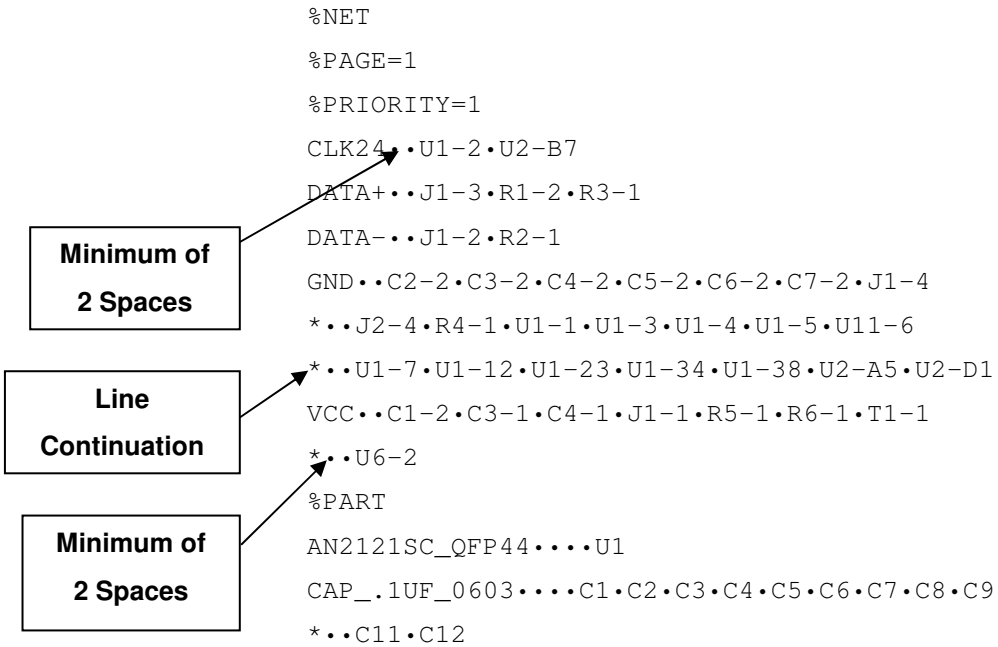
SPECIAL TOPICS

- CAD-SPECIFIC PROCEDURES
- HIGH-SPEED DESIGN RULES

3 CAD-Specific Procedures

3.1.1 Mentor Graphics – Expedition

3.1.1.1 Mentor Expedition Netlist Format



3.1.2 Mentor Graphics – PADS

3.1.2.1 Mentor PADS Netlist Format (must be .asc)

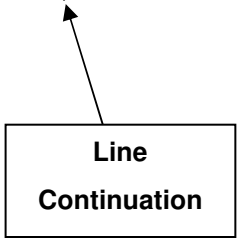
```
!PADS-POWERPCB-V5.0-MILS!
*PART*
U1·····AN2121SC_QFP44
C1·····CAP_.1UF_0603
C2·····CAP_.1UF_0603
C3·····CAP_.1UF_0603
C4·····CAP_.1UF_0603
C5·····CAP_.1UF_0603
C6·····CAP_.1UF_0603
C7·····CAP_.1UF_0603
C8·····CAP_.1UF_0603
C9·····CAP_.1UF_0603
C10····CAP_.1UF_0603
C11····CAP_.1UF_0603
C12····CAP_.1UF_0603
J1·····CONN_4PIN_USB
R1·····RES_1.5K_0402
R2·····RES_1.5K_0402
R3·····RES_1.5K_0402

*Net*
*Signal*·CLK24
U1.2·U2.B7
*Signal*·DATA+
J1.3·R1.2·R3.1
*Signal*·DATA-
J1.2·R2.1
*Signal*·GND
C2.2·C3.2·C4.2·C5.2·C6.2·C7.2·J1.4
J2.4·R4.1·U1.1·U1.3·U1.4·U1.5·U11.6
U1.7·U1.12·U1.23·U1.34·U1.38·U2.A5·U2.D1
*Signal*·VCC
C1.2·C3.1·C4.1·J1.1·R5.1·R6.1·T1.1
U6.2
*END*
```

3.1.3 Cadence – Allegro

3.1.3.1 Cadence Allegro Netlist Format

```
$PACKAGES
100TQFTP65•!•AN2121SC_QFP44•;•U1
SMD0603•!•CAP_.1UF_0603•;•C1•C2•C3•C4•C5•C6•C7•C8•C9,
C11•C12
CN_4PIN_USB•!•CONN_4PIN_USB•;•J1
SMD0402•!•RES_1.5K_0402•;•R1•R2•R3
$NETS
'CLK24'•;•U1.2•U2.B7
'DATA+'•;•J1.3•R1.2•R3.1
'DATA-'•;•J1.2•R2.1
•'GND'•;•C2.2•C3.2•C4.2•C5.2•C6.2•C7.2•J1.4,
J2.4•R4.1•U1.1•U1.3•U1.4•U1.5•U11.6,
U1.7•U1.12•U1.23•U1.34•U1.38•U2.A5•U2.D1
•'VCC'•;•C1.2•C3.1•C4.1•J1.1•R5.1•R6.1•T1.1,
U2.C1•U2.F7•U2.G3•U3.1•U5.2•U5.5•U6.1,
U6.2
$END
```



4 DESIGNER'S REFERENCE MATERIAL

4.1 APPENDIX C: CHECKLIST for ENGINEER / DESIGNER

Mechanical Spec.

Board laminate material spec, FR-4, FR-406, 4003, etc.

For large boards, are stiffeners required

Plug in cards, VME or compact PCI, etc., ground strips top and bottom for guides contact.

Fixed component locations

Floorplan available

Use of component tie downs if board is for high vibration environment like avionics

Maximum thickness and / or layer count

Mounting holes plated / non-plated. Nets for plated.

Place / route obstructs, including height restrictions.

Clearance requirements around connectors for mating half

Thermal considerations, heatsinks location & orientation, temperature sensitive components.

RF shielding used? Identification of sensitive circuit areas.

Bypassing components assigned, rules per device.

Board stack-up defined by ODA, Customer, or fabrication shop (preferred)

Controlled impedance requirements defined and verified against stack-up.

Planes assignments per layer, split planes allowed, local planes for specific devices.

Net classes defined.

Net properties defined.

Termination components present, optimal placement criteria for terminations.

Route topologies for specific circuit types, JTAG, Busses, LVDS, differential pairs, analog, power.

If diff pairs exist, edge coupled or broadside.

Vias tented or exposed.

Via walls required for sensitive signals

Fanout all BGA pins, including unused. If not fanned out there is better power to inner row pins of BGA, especially if using sub 1mm pitch devices.

Are there any high voltage areas, circuits requiring electrical isolation?

Through holes and vias buried or thermal ties.

Teardrops for thin traces at through hole connector pins

SMT in power circuits buried or thermal ties to surface planes.

Remove unused inner layer pads at Gerber out

ICT required, preferred and minimum spacing

Renumber reference designators required

Reference designators visible on silk for high density designs

Silkscreen functional label for connectors, switches and jumpers

4.2 APPENDIX D: ODA JOB NAMING CONVENTIONS

ANATOMY OF AN ODA JOB

4.3 APPENDIX E: PAPER SIZE CHART

U.S. paper sizes may be referred to in either of two ways: by size or by letter. Paper sizes begin with the standard 8.5" by 11" sheet, which is an A-Size sheet of paper. The larger sizes (B, C, etc.) are determined by doubling the smaller dimension. In doing this, the following sizes are obtained:

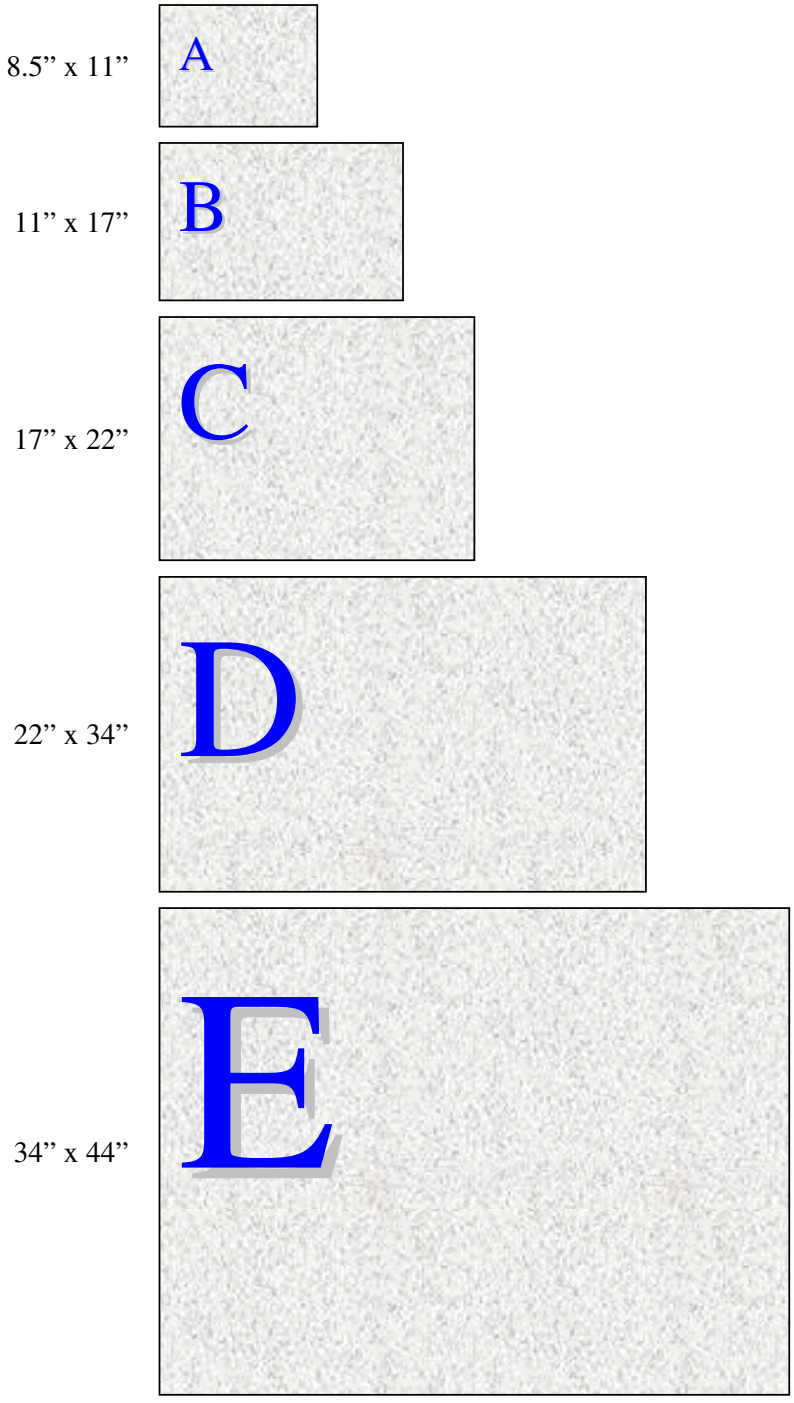


Figure 81: Paper Size Chart

4.4 APPENDIX F: ODA Part to Part Clearance Matrix

The following chart specifies the minimum clearance between surface-mounted components and other adjacent parts. All dimensions are in inches. See Notes for further dimensional requirements.

ODA Part to Part Clearance Matrix

	CHIP	CHIP	TANT	TANT	SO	SO	QFP	SOT	SOT	DPAK	DPAK	PLCC	SOJ	SOJ	BGA	DIP	DIP
CHIP	.015 .030	.025 .040	.035 .050	.050 .075	.030 .040	.025 .040	.025 .040	.030 .040	.025 .040	.050 .075	.050 .075	.035 .050	.035 .050	.025 .050	.150 .200	.050 .075	.050 .075
CHIP	.025 .040	.020 .040	.050 .075	.025 .050	.025 .040	.025 .040	.025 .040	.030 .040	.025 .040	.050 .075	.025 .050	.030 .050	.030 .050	.025 .050	.150 .200	.065 .100	.065 .100
TANT.	.035 .050	.050 .075	.025 .050	.050 .075	.050 .075	.025 .050	.040 .075	.050 .075	.050 .075	.075 .100	.075 .100	.075 .100	.075 .100	.050 .075	.150 .200	.050 .075	.050 .075
TANT	.050 .075	.025 .050	.050 .075	.025 .050	.050 .075	.035 .050	.040 .075	.050 .075	.050 .075	.060 .100	.060 .100	.075 .100	.075 .100	.050 .075	.150 .200	.065 .100	.065 .100
SO	.030 .040	.025 .040	.050 .075	.050 .075	.025 .050	.050 .075	.050 .050	.030 .050	.040 .075	.075 .100	.075 .100	.100 .100	.100 .100	.075 .100	.150 .200	.050 .075	.050 .075
SO	.025 .040	.025 .040	.025 .050	.035 .050	.050 .075	.025 .025	.050 .075	.040 .075	.030 .050	.075 .100	.075 .100	.100 .100	.100 .100	.075 .100	.150 .200	.050 .075	.100 .100
QFP	.025 .040	.025 .040	.040 .075	.040 .075	.050 .050	.050 .075	.050 .050	.030 .050	.040 .075	.075 .100	.075 .100	.100 .100	.100 .100	.075 .100	.150 .200	.100 .100	.100 .100
SOT	.030 .040	.030 .040	.050 .075	.050 .075	.030 .050	.040 .075	.030 .050	.025 .035	.050 .075	.075 .100	.050 .075	.050 .100	.050 .100	.050 .075	.150 .200	.050 .075	.050 .075
SOT	.025 .040	.025 .040	.050 .075	.050 .075	.040 .075	.030 .050	.040 .075	.050 .075	.025 .035	.075 .100	.050 .075	.050 .100	.050 .100	.050 .075	.150 .200	.065 .100	.065 .100
DPAK	.050 .075	.050 .075	.075 .100	.060 .100	.075 .100	.075 .100	.075 .100	.075 .100	.075 .100	.100 .150	.150 .150	.150 .150	.150 .150	.100 .150	.150 .200	.100 .150	.100 .150
DPAK	.050 .075	.025 .050	.075 .100	.060 .100	.075 .100	.075 .100	.075 .100	.075 .100	.050 .075	.150 .150	.100 .150	.150 .150	.150 .150	.100 .150	.150 .200	.150 .200	.150 .200
PLCC	.035 .050	.030 .050	.075 .100	.075 .100	.100 .100	.100 .100	.100 .100	.050 .100	.050 .100	.150 .150	.150 .150	.125 .125	.125 .125	.125 .125	.150 .200	.100 .200	.200 .200
SOJ	.035 .050	.030 .050	.075 .100	.075 .100	.100 .100	.100 .100	.100 .100	.050 .100	.050 .100	.150 .150	.150 .150	.125 .125	.050 .075	.125 .125	.150 .200	.050 .075	.100 .200
SOJ	.025 .050	.025 .050	.050 .075	.050 .075	.075 .100	.075 .100	.075 .100	.050 .075	.050 .075	.100 .150	.100 .150	.100 .125	.125 .125	.050 .075	.150 .200	.125 .200	.200 .200
BGA	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200	.150 .200
THRU	.050 .075	.065 .100	.050 .075	.065 .100	.050 .075	.050 .075	.100 .100	.050 .075	.065 .100	.100 .150	.150 .200	.100 .200	.050 .075	.125 .200	.150 .200	.100 .100	.100 .100
THRU	.050 .075	.065 .100	.050 .075	.065 .100	.050 .075	.100 .100	.100 .100	.050 .075	.065 .100	.100 .150	.150 .200	.200 .200	.100 .200	.200 .200	.150 .200	.100 .100	.100 .100

Standard Density (preferred minimum)

HIGH DENSITY (absolute minimum)

4.5 APPENDIX G: FABRICATION DRAWING REQUIREMENTS

4.5.1 Drafting Standards

All drawings must follow industry-accepted standards of drafting. They should communicate the essential information quickly to readers unfamiliar with the contents of the document. ODA drafting practices include the following guidelines:

1. The 0-0 point must be clearly marked.
2. Dimensioning arrows must not cross other dimensioning lines.
3. Alternate views of an object will be placed on the page relative to the central view. In other words, the top view will be placed above the central view, the right-hand view to the right, etc. See the accompanying figure for an example.

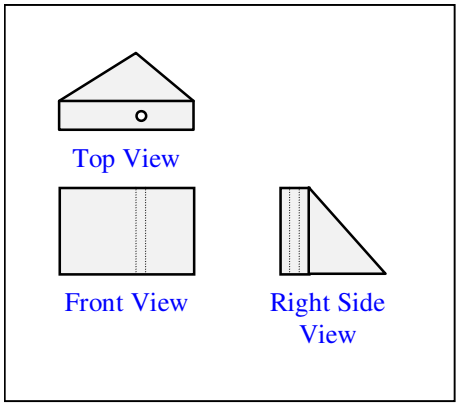
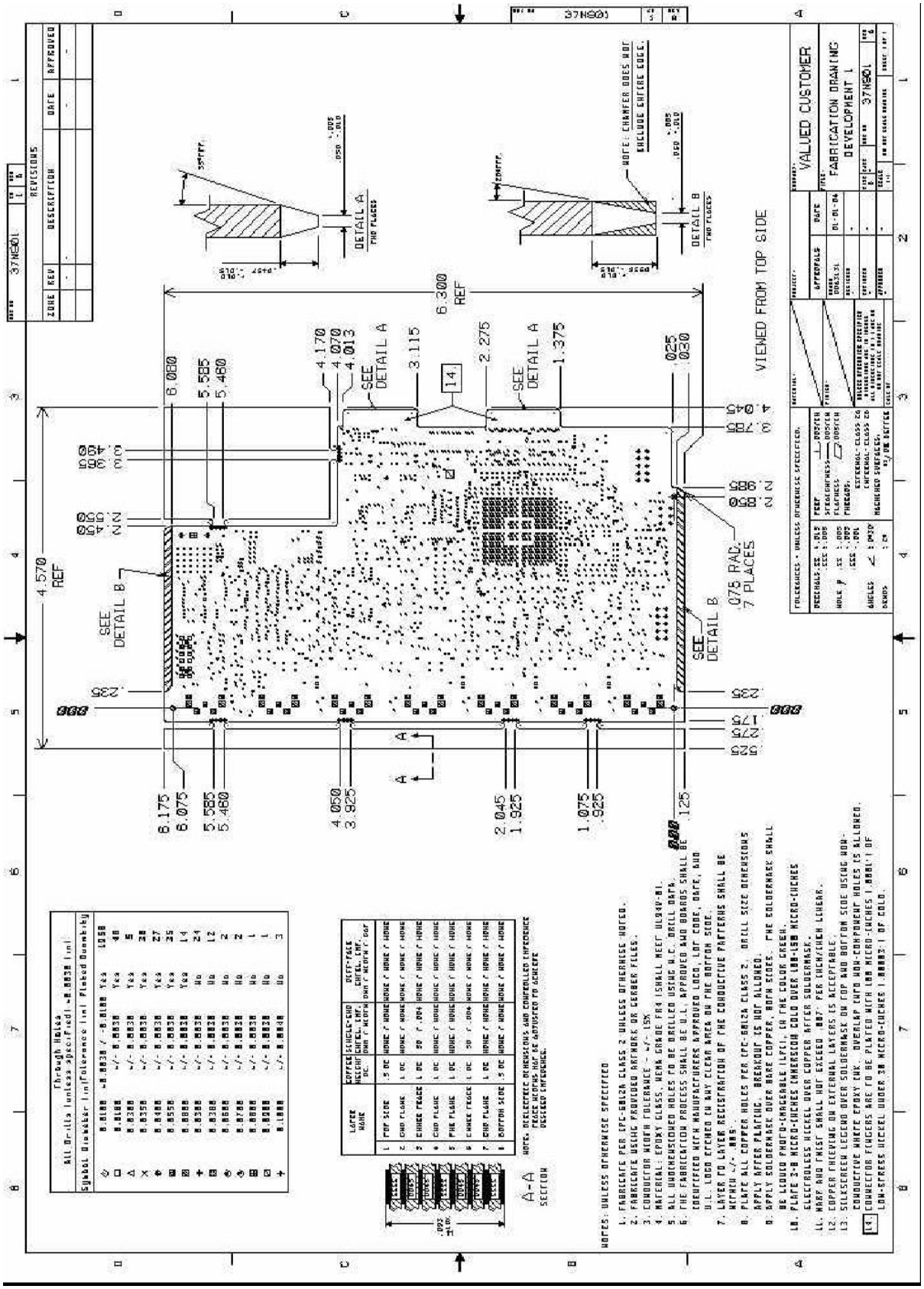


Figure 82: Standard Drafting Views

4. Object views or details will be given captions, centered and underlined beneath the object or view.
5. Callouts will have reference arrows drawn at 45-degree angles.
6. Dimensions given purely for reference must be so noted with the word, REF, beneath or after the number.

The following figure illustrates a typical fabrication drawing and its various sections.


VIEWED FROM TOP SIDE
DETAIL A
DETAIL B
SEE DETAIL A
SEE DETAIL B
4.570 REF
6.300 REF
6.050
5.585
5.480
4.170
4.070
4.013
3.115
2.275
1.375
.075 RAD. 7 PLACES
VALUED CUSTOMER
FABRICATION DRAWING
DEVELOPMENT 1
37NS01
A-A
SECTION
NOTES: UNLESS OTHERWISE SPECIFIED

4.6 APPENDIX H: AWG (American Wire Gauge) CHART

Use the following table to determine drill sizes for bare wires that attach to a PCB.

Table 12: Drill Chart for Bare Wire

AWG	DIA (MILS)	DIA (MM)	DRILL (MILS)
36	5	.127	15
35	5.6	.142	15
34	6	.152	15
33	7	.178	15
32	8	.208	20
31	9	.228	20
30	10	.254	20
29	11	.280	20
28	13	.330	25
27	14	.356	25
26	16	.406	25
25	18	.457	30
24	20	.508	30
23	23	.584	35
22	25	.635	35
21	28	.711	40
20	32	.813	40
19	36	.914	45
18	40	1.016	50
17	45	1.143	55
16	50	1.270	60
15	57	1.448	70
14	64	1.626	75
13	72	1.829	80
12	81	2.057	90
11	90	2.286	100
10	102	2.590	110
9	114	2.896	125
8	128	3.251	140
7	144	3.658	155
6	162	4.115	175
5	182	4.623	190
4	204	5.182	215
3	229	5.817	240
2	258	6.553	270
1	289	7.340	300
0	325	8.255	335

4.7 APPENDIX I: NUT/BOLT SIZES AND CLEARANCES

PC boards have had many different parts mounted to them in the past. And while boards can support only a small amount of weight and torque, a great many parts can be attached with standard machined hardware, such as nuts, bolts, screws and washers.

In order for this hardware to mount the parts without shorting out circuitry or causing other problems, the designer must allow fairly large clearance areas on the board. The following chart shows the sizes and clearances for a variety of small machined mounting hardware. Use this information to create keepout areas, pads and fill areas on designs that require hardware to mount their parts.

Table 13: Mounting Hardware Chart

H/W Style	0-80			2-56			4-40		
Parts	Dims	Pad	Clear (Drill)	Dims	Pad	Clear (Drill)	Dims	Pad	Clear (Drill)
Head:									
Flat	.119	.130	.145	.172	.180	.195	.225	.235	.250
Pan	.116	.125	.140	.167	.180	.195	.219	.230	.245
Socket	N/A	—	—	.140	.150	.165	.185	.200	.215
Threads	.060	—	(.070)	.086	—	(.100)	.112	—	(.120)
Washer:									
Flat	.188	.200	.215	.250	.260	.275	.320	.330	.345
Ext. Tooth	N/A	—	—	N/A	—	—	.260	.270	.285
Int. Tooth	N/A	—	—	.200	.210	.225	.270	.280	.295
Split (C)	.119	.130	.145	.172	.180	.195	.209	.220	.235
Nut:									
Point-Point	.180	.190	.205	.217	.230	.245	.289	.300	.315
Flat-Flat	.161	.190	.205	.188	.230	.245	.250	.300	.315

H/W Style	6-32			8-32			10-32		
Parts	Dims	Pad	Clear (Drill)	Dims	Pad	Clear (Drill)	Dims	Pad	Clear (Drill)
Head:									
Flat	.279	.290	.305	.332	.340	.355	.385	.395	.410
Pan	.270	.280	.295	.322	.330	.345	.373	.385	.400
Socket	.266	.275	.290	.270	.280	.295	.313	.325	.340
Threads	.138	—	(.150)	.164	—	(.175)	.190	—	(.200)
Washer:									
Flat	.390	.400	.415	.390	.400	.415	.577	.585	.600
Ext. Tooth	.320	.330	.345	.381	.390	.405	.410	.420	.435
Int. Tooth	.295	.305	.320	.340	.350	.365	.381	.390	.405
Split (C)	.250	.260	.275	.293	.305	.320	.334	.345	.360
Nut:									
Point-Point	.361	.370	.385	.397	.405	.420	.433	.445	.460
Flat-Flat	.312	.370	.385	.344	.405	.420	.375	.445	.460

NOTE: Pad and clear areas for **Standoffs** should be the same as those for Nuts in these charts.

4.8 APPENDIX J: TRACE WIDTH CURRENT CAPACITY

The following tables show the minimum line widths for various current capacities at four different temperature rises and for three different copper thicknesses.

Please note that normally you would use the data in the 30° column, unless the design requirements call for tighter restrictions. In addition, keep in mind that the capacity of external layers depends on the final thickness of the traces, which is the copper thickness plus any additional plating.

These calculations have been derived from IPC Standard 2221A-6.2, which will be updated upon the release of IPC 2152. Please note that the internal trace width calculations are conservative, that is, the given trace width *should* be capable of handling higher current than specified. (IPC 2152 will provide more accurate results based on more thorough testing with a greater number of variables that affect the results.)

The IPC 2221A formula, solving for current capacity (I), is:

$$I = k\Delta T^{0.44} A^{0.725}$$

Where,

I = Current in Amperes
A = Cross-sectional area in sq. mils
ΔT = Temperature rise in ºC
k = 0.048 (external layers), 0.024 (internal layers)

Cross-sectional area (A) is the trace width (w) multiplied by the copper thickness (t). Copper thicknesses for the three types given are:

- 0.5 oz. = 0.7Mils
- 1.0 oz. = 1.4Mils
- 2.0 oz. = 2.8Mils

Rather than asking, “How many Amps will this trace carry?” designers are more likely to face the question, “What size trace do I need in order to carry *N* Amps?” To answer this question, we need to solve for w instead of I. This is done in the following formula:

$$w = \frac{\sqrt[0.725]{\frac{I}{k\Delta T^{0.44}}}}{t}$$

In the following two charts, trace sizes of less than 1 Mil (0.001") are omitted, along with trace sizes greater than 1000 Mil (1.0").

In addition to these formulas and charts, other resources for determining trace size for a given current capacity are the graphs given in IPC standard 2221A-6.2 (p. 41) and the trace size calculator program, PCTEMP, found at www.ultracad.com.

Table 14: Trace Current Capacity Per IPC Standards – External Layers

	TEMPERATURE RISE											
	10° C			20° C			30° C			45° C		
Copper Thickness / Current	0.5 oz.	1 oz.	2 oz.	0.5 oz.	1 oz.	2 oz.	0.5 oz.	1 oz.	2 oz.	0.5 oz.	1 oz.	2 oz.
.25 A	3	1		2	1		1			1		
.40 A	5	3	1	3	2		3	1		2		
.50 A	7	4	2	5	2	1	4	2	1	3	1	
.75 A	13	6	3	8	4	2	6	3	2	5	3	1
1.0 A	20	10	5	13	6	3	10	5	3	8	4	2
1.5 A	36	18	9	23	12	6	18	9	5	14	7	4
2.0 A	55	28	14	36	18	9	27	14	7	21	11	5
2.5 A	77	38	19	49	25	12	38	19	10	30	15	7
3.0 A	101	50	25	65	32	16	50	25	13	39	19	10
3.5 A	127	63	32	82	41	20	63	32	16	49	24	12
4.0 A	155	77	39	100	50	25	77	38	19	59	30	15
5.0 A	215	108	54	139	69	35	107	53	27	83	41	21
6.0 A	282	141	71	182	91	45	140	70	35	109	54	27
7.5 A	393	197	98	253	127	63	196	98	49	151	76	38
10.0 A	603	301	151	388	194	97	300	150	75	232	116	58
12.5 A	840	420	210	540	270	135	418	209	104	323	161	81
15.0 A		550	275	709	354	177	547	274	137	423	212	106

Table 15: Trace Current Capacity Per IPC Standards – Internal Layers

	TEMPERATURE RISE											
	10° C			20° C			30° C			45° C		
Copper Thickness / Current	0.5 oz.	1 oz.	2 oz.	0.5 oz.	1 oz.	2 oz.	0.5 oz.	1 oz.	2 oz.	0.5 oz.	1 oz.	2 oz.
.25 A	12	6	3	7	4	2	5	3	1	4	2	1
.40 A	23	12	6	14	7	3	10	5	3	8	4	2
.50 A	31	16	8	19	9	5	14	7	4	10	5	3
.75 A	54	27	14	32	16	8	24	12	6	18	9	4
1.0 A	80	40	20	49	24	12	35	18	9	26	13	7
1.5 A	139	70	35	83	42	21	62	30	15	46	23	11
2.0 A	205	103	51	123	61	31	91	45	23	67	34	17
2.5 A	278	139	70	166	83	42	123	62	31	91	46	23
3.0 A	357	178	89	213	107	53	158	79	40	117	58	29
3.5 A	440	220	110	263	132	66	195	97	49	144	72	36
4.0 A	528	264	132	316	158	79	234	117	58	173	86	43
5.0 A	715	358	179	428	214	107	316	158	79	234	117	59
6.0 A	916	458	230	548	274	137	406	203	101	300	150	75
7.5 A		621	310	742	371	186	549	275	137	407	203	101
10.0 A		918	459		549	274	812	406	203	601	300	150
12.5 A			622		744	372		550	275	814	407	204
15.0 A			797		953	477		705	353		522	261

4.9 APPENDIX K: ASSEMBLY PROCESSES

Part of a designer's professional development should be to learn as much as possible about the activities that go before and come after the layout process. And with today's highly complex designs, the assembly process has grown in importance, and has become a major concern for designers.

A basic understanding of the assembly step is to know the various ways in which the components are attached to the board. These methods depend upon the type of components (thru-hole or SMD) and their location (one side or two sides.) The combinations of component types and locations are as follows, along with the associated assembly methods:

1. Thru-hole, one side	Kit, Auto Insert, Semi-Auto Insert, Hand Insert, Wave Solder, Clean, Post-Wave Assembly, Test
2. SMD, one side	Kit, Print Solder Paste, Auto Place, Reflow, Clean, Test
3. Mixed, one side	Kit SMD Parts, Print Solder Paste, Auto Place Reflow, Clean, Kit Thru-Hole Parts, Auto/Hand Insert, Wave Solder, Clean, Test
4. SMD, two sides	Kit Top-Side SMD Parts, Print Solder Paste, Auto Place, Reflow, Clean, Kit Bottom-Side SMD Parts, Print Solder Paste, Auto Place, Reflow, Clean, Test
5. Thru-hole, one side; SMD, two sides	Kit Top-Side SMD Parts, Print Solder Paste, Auto Place, Reflow, Clean, Kit Bottom-Side SMD Parts, Print Solder Paste, Auto Place, Reflow, Clean, Kit Thru-Hole Parts, Auto/Hand Insert, Wave Solder, Clean, Test.

There are many more assembly issues that affect the PCB designer. As they become documented they will be added to this section. Designers, however, are encouraged to continually seek out information that will enable them to increase their ability to serve the customer.

4.10 APPENDIX L: STANDARD REFERENCE DESIGNATOR PREFIXES

Table 16: Reference Designator Prefixes

Prefix	Part	Abbreviation
U	Integrated Circuit	IC
C	Capacitor	CAP
R	Resistor	RES
J	Connector	CONN
P	Connector	CONN
L	Choke (or Inductor)	IND
D	Diode (or LED)	
CR	Diode (or LED)	
Q	Transistor	TRANS
B	Battery	
F	Fuse	
X	Crystal	XTAL
K	Relay	
SW	Switch	SW
T	Transformer	XFMR
TP	Testpoint	TP
W	Jumper	JMP, JPR
JP	Jumper	JMP, JPR

4.11 APPENDIX M: Fraction/Decimal/MM Equivalents

FRACTIONS	DECIMALS	MM
1/64	.015625	.397
1/32	.031250	.794
3/64	.046875	1.588
1/16	.062500	1.191
5/64	.078125	1.984
3/32	.093750	2.381
7/64	.109375	2.778
1/8	.125000	3.175
9/64	.140625	3.572
5/32	.156250	3.969
11/64	.171850	4.366
3/16	.187500	4.763
13/64	.203125	5.159
7/32	.218750	5.556
15/64	.234375	5.953
1/4	.250000	6.350
17/64	.265625	6.747
9/32	.281250	7.144
19/64	.296875	7.541
5/16	.312500	7.938
21/64	.328125	8.334
11/32	.343750	8.731
23/64	.359375	9.128
3/8	.375000	9.525
25/64	.390625	9.922
13/32	.406250	10.319
27/64	.421875	10.716
7/16	.437500	11.113
29/64	.453125	11.509
15/32	.468750	11.906
31/64	.484375	12.303
1/2	.500000	12.700
33/64	.515625	13.097
17/32	.531250	13.494
35/64	.546875	13.891
9/16	.562500	14.288
37/64	.578125	14.684
19/32	.593750	15.081
39/64	.609375	15.475
5/8	.625000	15.875
41/64	.640625	16.272
21/32	.656250	16.669
43/64	.671875	17.066
11/16	.687500	17.463
45/64	.703125	17.859
23/32	.718750	18.256
47/64	.734375	18.653
3/4	.750000	19.050
49/64	.765625	19.447
25/32	.781250	19.844
51/64	.796875	20.241
13/16	.812500	20.638
53/64	.828125	21.034
27/32	.843750	21.431
55/64	.859375	21.828
7/8	.875000	22.225
57/64	.890625	22.622
15/16	.937500	23.813
1	1.000000	25.400

APPENDIX N: Two-Layer PCBs: Power Stitching

On a two-layer PCB, the designer must be concerned with proper power and ground distribution throughout the whole circuitry. This means that the main power arteries must be quite thick, multiple vias must be used to get the power to the other side of the board and the power must be "stitched" in several places to maintain constant voltage. **Figure 83** illustrates proper power distribution on a two-layer board.

The time to think about power stitching is at the beginning of the design, at least prior to routing signal traces. Start with more than enough trace thickness, vias and stitching, and then if the design gets too tight to finish, reduce some of the power connections. It is easier to subtract power stitching than it is to add it after the fact.

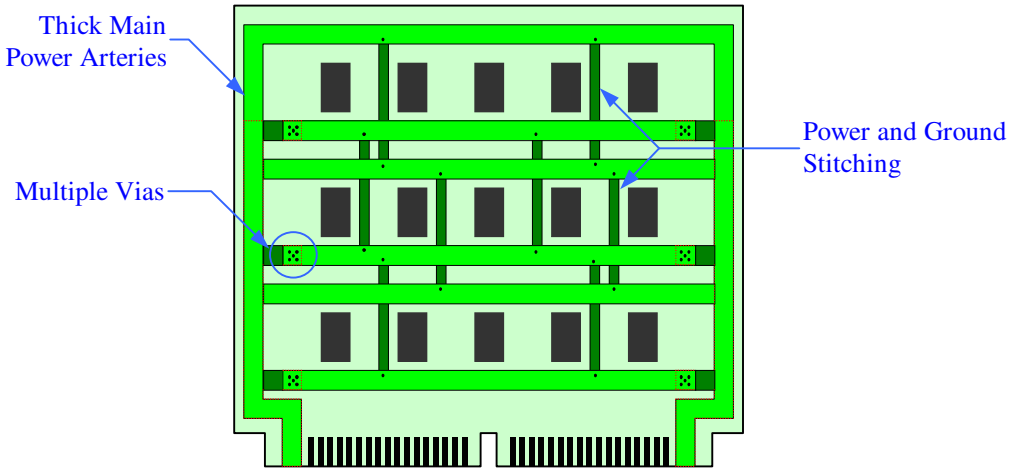


Figure 83: Power Stitching, Two-Layer PCB's

4.12 APPENDIX O: Surface Tension Model

The critical consideration when selecting components for suspended bottom side reflow is the surface-tension-to-weight ratio. To determine whether the surface tension of a given device is adequate to sustain its weight during a suspended second pass reflow operation, one should apply a modeling tool which is based on surface tension theory and static force balance. According to the surface tension theory, the liquid surface exerts tension upon adjacent portions of the surface or upon other objects that are in contact with the liquid. The tension acts in the plane of the surface, and its magnitude per unit length is defined as surface tension τ (tau). As a result, the force that acts on a lead is equal to the surface tension multiplied by the length of the lead in contact with the solder. The model requires lead length, lead width, heel radius, and number of leads for the calculation of total contact length. To use the model, substitute the variables from your component specification into the following formulas.

Example

Component Type: 0.5mm PQFP, 208 leads

Component Weight (W) = 1.6 gm

Lead Length (L) = 0.5 mm

Lead Width (b) = 0.2 mm

Heel Radius (R) = 0.2 mm

Number of Leads (N) = 208

Surface Tension of Sn/Pb, 63:37 (τ) = 462 dynes/cm (constant for this solder alloy)

Acceleration Constant (a) = 981 cm/sec^2

Gull Wing Formulas

Contact Length (P) = $\{b + (L - R) + (\pi R/4)\} \times 2 \times N = 273.35$ mm

Predicted Weight (PW) = $(P/10) \times \tau \times (1/a) = 12.87$ gm

Note: Formula for calculating contact length (P) is lead configuration specific (i.e. gull wing vs. J-lead vs. butt joint).

This example indicates that the surface tension developed from 208 leads of a 0.5mm PQFP can support 12.87 grams of component weight. A safety factor of at least 2X is recommended when using this formula. With an actual component weight of 1.6 gm, this example should process favorably unless disturbed during reflow, or solder quality was poor to start with.

4.13 APPENDIX P: Electrical Conductor Spacing

Table 6-1 Electrical Conductor Spacing

Voltage Between Conductors (DC or AC Peaks)	Minimum Spacing						
	Bare Board				Assembly		
	B1	B2	B3	B4	A5	A6	A7
0-15	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]
16-30	0.05 mm [0.00197 in]	0.1 mm [0.0039 in]	0.1 mm [0.0039 in]	0.05 mm [0.00197 in]	0.13 mm [0.00512 in]	0.25 mm [0.00984 in]	0.13 mm [0.00512 in]
31-50	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	0.6 mm [0.024 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.4 mm [0.016 in]	0.13 mm [0.00512 in]
51-100	0.1 mm [0.0039 in]	0.6 mm [0.024 in]	1.5 mm [0.0591 in]	0.13 mm [0.00512 in]	0.13 mm [0.00512 in]	0.5 mm [0.020 in]	0.13 mm [0.00512 in]
101-150	0.2 mm [0.0079 in]	0.6 mm [0.024 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
151-170	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	3.2 mm [0.126 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
171-250	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	6.4 mm [0.252 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.4 mm [0.016 in]
251-300	0.2 mm [0.0079 in]	1.25 mm [0.0492 in]	12.5 mm [0.4921 in]	0.4 mm [0.016 in]	0.4 mm [0.016 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]
301-500	0.25 mm [0.00984 in]	2.5 mm [0.0984 in]	12.5 mm [0.4921 in]	0.8 mm [0.031 in]	0.8 mm [0.031 in]	1.5 mm [0.0591 in]	0.8 mm [0.031 in]
> 500 See para. 6.3 for calc.	0.0025 mm /volt	0.005 mm /volt	0.025 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt	0.00305 mm /volt

B1 - Internal Conductors
B2 - External Conductors, uncoated, sea level to 3050 m [10,007 feet]
B3 - External Conductors, uncoated, over 3050 m [10,007 feet]
B4 - External Conductors, with permanent polymer coating (any elevation)
A5 - External Conductors, with conformal coating over assembly (any elevation)
A6 - External Component lead/termination, uncoated, sea level to 3050 m [10,007 feet]
A7 - External Component lead termination, with conformal coating (any elevation)

Source: IPC2221A